Final Program and Abstracts

Topical Workshop on Heterostructure Microelectronics (TWHM '00)

August 20 to 23, 2000

Kyoto Research Park
Kyoto, Japan

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Nippon Sheet Glass Foundation for Material Science and Engineering
The Murata Science Foundation

Preface

Welcome to the 2000 Topical Workshop on Heterosructure Microelectronics (TWHM'00). The Workshop addresses technical issues for further progress of the heterostructure high-speed device technology and provides a forum for international collaboration. Since 1994, when this Workshop began in Susono, it was followed by another successful meetings at Sapporo and Hayama-machi. This year, the forth TWHM is being held in Kyoto, the ancient capital of Japan. Emphasis is placed on practical and mature devices that are expected to play key roles in the coming multi-media era.

The sessions contains a variety of contributions on devices, materials, circuits and systems. The technologies employed are based on heterostructure bipolar transistors, heterostructure field effect transistors and novel devices, and make use of variety of heterostructure material systems including III-Vs (e.g. GaAs, InP, and related compounds), group IV semiconductors (e.g. SiGe), and wide bandgap semiconductors (e.g. III-V Nitrides). The program committee invited exciting and stimulating leaders in the heterostructure technology field. Emphasis is placed on the GaN and SiGe devices to discuss the prospect of their actual applications.

We would like to take this opportunity to thank the workshop committee members of TWHM '00 for soliciting papers and arranging the excellent program. The financial support made by the followings are also greatly appreciated; Asian Office of Aerospace Research and Development/Air Force Office of Scientific Research (AOARD/AFOSR), Nippon Telegraph and Telephone Corporation (NTT), Matsushita Electronics Corporation, NEC Corporation, Mitsubishi Electric Corporation, Toshiba Corporation, Oki Electric Industry Corporation, Nippon Sheet Glass Foundation for Material Science and Engineering, and The Murata Science Foundation. We would like to thank Technical Group on Electron Devices, Electronics Society, The Institute of Electronics, Information and Communication Engineers for the co-sponsorship. Technical sponsorship by IEEE Electron Devices Society and the Japan Society of Applied Physics has also been instrumental in the organization of this workshop.

Finally, we hope you will find this year's Workshop useful and stimulating and encourage you to share your experience with others in order to contribute the successful expansion of the field of Heterostructure Microelectronics.

Takashi Mizutani	Burhan Bayraktaroglu	Ulf Konig
Workshop Co-Chair	Workshop Co-Chair	Workshop Co-Chair

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9:00 **Opening Remarks**
T. Mizutani **(Nagoya University)**
B. Bayraktaroglu **(ANADIGICS, Inc.)**
U. Konig **(DaimlerChrysler)**

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Chair persons S. Takamiya, H. Tokuda

11:00~11:20 **Coffee Break**

Session 2 HFETs Monday, August 21 (11:20~12:20)

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Session 3 Wide Bandgap Devices Monday, Aug. 21 (13:50~15:45)

Chair persons Y. Miyamoto, Y. Ohta

Session 4 Novel Devices — Monday, August 21 (16:05~17:20)

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12:30~ 18:00 Excursion with Lunch

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Session 7 SiGe HBTs & FETs Wednesday, August 23 (9:00~10:15)

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Gate and Recess Engineering for Ultrahigh-Speed InP-Based HEMTs

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*NTT Photonics Laboratories and **NTT Basic Research Laboratories*
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InP-based HEMTs are the fastest transistors available at present and will be so for the foreseeable future. Indeed, a cutoff frequency (f_T) of over 350 GHz has been reported by two groups [1,2]. The gate recess - the uncapped region adjacent to the gate electrode - plays an important role in device characteristics and reliability. In this paper, the impact of the lateral depth of the gate recess, i.e., the recess length (L_{side}), on the characteristics of ultrashort-gate HEMTs, and the role of gate recess plays in reliability are discussed.

The gate fabrication was optimized to reduce the gate length (L_g) [1]. The bottom of the T-shaped gate was patterned by e-beam lithography, and the top was then patterned by a different lithography. A fullerene-incorporated nanocomposite resist was employed for the e-beam lithography. The fullerene molecules, which fill the space between resist molecules, prevent the patterns from degrading during development and etching [3]. The enhanced etching resistance enables us to reduce the resist thickness, which can improve the resolution. Two-step (TS) recess etching, which defines the gate length as it is patterned, was used [4]. The SEM photograph in Fig. 2 shows the cross section of a fabricated 30-nm gate. The recess length was controlled by the wet-chemical recess etching time. Samples having L_{side}'s ranging from 50 to 400 nm were prepared.

The delay time, given by $1/2\pi f_T$, consists of the intrinsic delay (L_g/v_s) and the extrinsic delay (τ_{ex}), which is independent of L_g [4]. The L_{side} dependence of f_T can therefore be explained by the difference in τ_{ex}. An expanded effective gate length (ΔL) and a carrier charging through C_{gd}, and the parasitic resistance (R_s, R_d) are the sources of τ_{ex} at small L_g [7]:

$$\tau_{ex} = \frac{\Delta L}{v_s} + \frac{C_{gd}}{g_{m0}}\{1 + (g_{m0} + g_{d0})(R_s + R_d)\}. \qquad (1)$$

Figure 3 shows the L_g dependence of f_T for a TS-recess gate and a conventional gate (i.e., the gate metal is deposited on the InP etch stopper [5]). The trend of L_g versus f_T is fitted by a common v_s of 2.7 x 10^7 cm/s for both structures and a different τ_{ex}; 0.28 ps for the TS-recess gate and 0.38 ps for the conventional one. The longer τ_{ex} for the conventional gate is ascribed to the spread of gate metal into the recess groove, which results in longer ΔL.

The conventional wisdom with regard to the gate recess is that a wide recess enables us to improve breakdown voltage and reduce feedback capacitance (C_{gd}) [5]. A wide recess is, however, known as a cause of large parasitic resistance. This penalty arises because the exposure of an undoped layer causes carrier depletion in the recess region (n_{ss}). Hence, the optimized L_{side} closely depends on the magnitude and stability of n_{ss}. The InP etch-stop layer enables us to widen L_{side} due to its stable recess surface [6].

Figure 4 shows the cutoff frequency (f_T) and the maximum transconductance ($g_{m,max}$) of 30-nm-gate HEMTs as a function of L_{side}. Though $g_{m,max}$ decreases monotonically as L_{side} is increased from 120 to 400 nm, the f_T has a peak at L_{side} of 260 nm. These results also indicate the influence of τ_{ex} on f_T; that is, longer L_{side} gives smaller C_{gd}, but larger R_s and R_d. Therefore, f_T has a peak at the L_{side} such that the second term of (1) is minimized. As shown in Fig. 5, the highest f_T, i.e., 368 GHz, is achieved at L_{side} = 260 nm.

Since the intrinsic delay L_g/v_s is estimated to be 0.11 ps at L_g = 30 nm, τ_{ex} is the principal factor limiting f_T. Therefore, further improvement in f_T will be realized by eliminating parasitic components ΔL, C_{gd}, R_s and R_d in (1).

Finally, the influence of L_{side} on reliability is examined. Each sample (L_g: 100 nm) was stored in nitrogen ambient at 195°C, and a drain voltage of 1.5 V and a gate voltage of 0.2 V were applied for 200h. The ΔR_s and ΔR_d, namely, increases in R_s and R_d, were observed for all samples. Since ΔR_s depends on the carrier supply layer material [8], the inactivation of Si donors in the InAlAs layer is a possible cause of ΔR_s. Regarding R_d, the ratio $\Delta R_d/\Delta R_s$ is plotted in Fig. 6 as a function of L_{side}. The plot indicates that smaller L_{side} causes damage that is more localized on the drain side. It suggests that the principal cause of ΔR_d becomes weaker with increasing L_{side}, or, at least, ΔR_d is less influenced by L_{side}.

In conclusion, the impact of gate and gate-recess size on device characteristics was studied for InP-based HEMTs. The f_T of 30-nm-gate HEMTs is currently limited by the extrinsic delay time. The InP recess surface allows us to extend the recess region without significant parasitic resistance, and an appropriate recess length, which depends on both the feedback capacitance and parasitic resistance, improves f_T particularly in short-gate HEMTs. Bias and temperature stress tests indicate that the gate recess helps relax the one-sided increase in the drain resistance.

The authors thank T. Tamamura for his help with the e-beam lithography and H. Yokoyama for crystal growth. They are very grateful to Y. K. Fukai, T. Enoki, D. Xu and Y. Umeda for fruitful discussions.

1. T. Suemitsu et al., IEDM (1998) 223.
2. A. Endoh et al., presented in IPRM (2000).
3. T. Ishii et al., Appl. Phys. Lett., 70 (1997) 1110.
4. T. Suemitsu et al., Jpn. J. Appl. Phys., 37 (1998) 1365.
5. T. Enoki et al., Jpn. J. Appl. Phys., 37 (1998) 1359.
6. G. Meneghesso et al., IEDM (1998) 227.
7. P. J. Tasker et al., IEEE Electron Device Lett., 10 (1989) 291.
8. Y. Fukai et al., submitted to TWHM (2000).

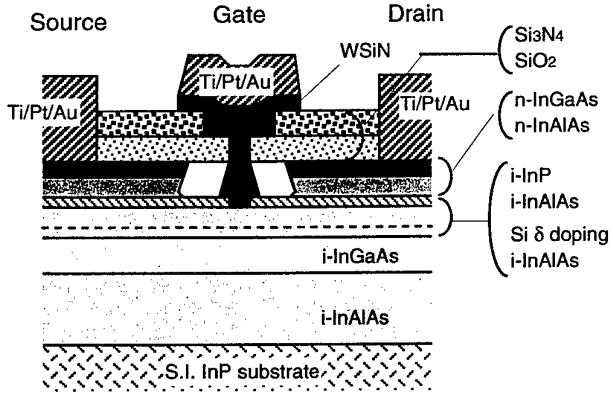

Fig. 1: Schematic cross section of a two-step recess gate HEMT. All epitaxial layers were grown by MOCVD and are lattice-matched to InP substrates.

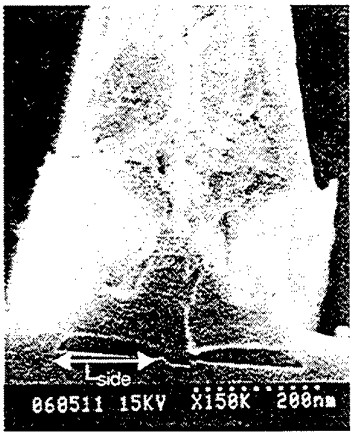

Fig. 2: Scanning electron microscope photograph of a 30-nm-gate HEMT. Lateral depth of the gate recess is defined as recess length (L_{side}).

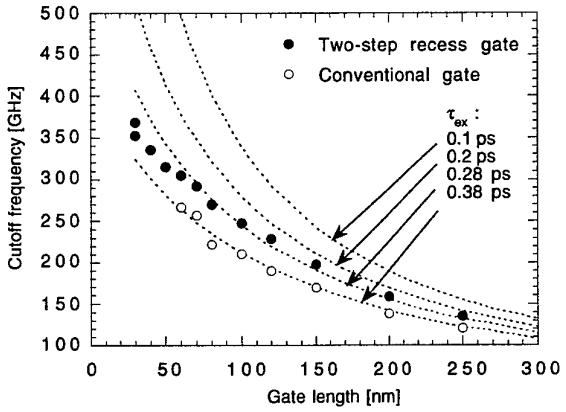

Fig. 3: Gate length (L_g) dependence of cutoff frequency (f_T) of two-step recess and conventional gate HEMTs. Dotted curves were calculated by $f_T = 1/[2\pi(\tau_{ex} + L_g/v_s)]$ with $v_s = 2.7 \times 10^7$ cm/s.

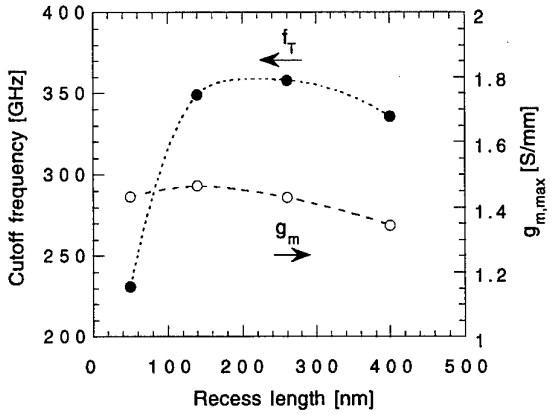

Fig. 4: Recess length (L_{side}) dependence of cutoff frequency (f_T) and maximum transconductance ($g_{m,max}$) of a 30-nm-gate HEMT. The f_T has its peak at the L_{side}, such that the second term of eq.(1) is minimized.

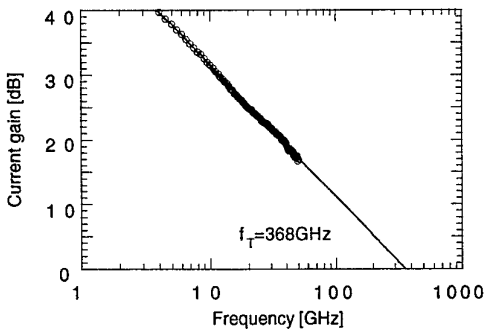

Fig. 5: Current gain of a 30-nm-gate HEMT (L_{side}: 260 nm). The -6 dB/octave line yields a cutoff frequency (f_T) of 368 GHz. V_{ds} = 0.6 V and V_{gs} = 0.15 V. Total gate width is 100 μm.

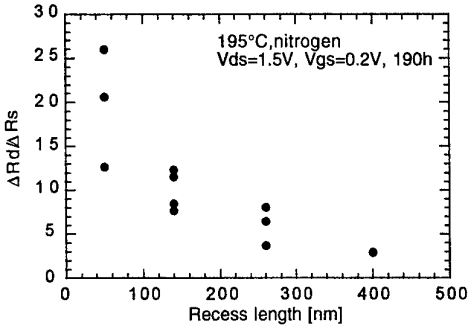

Fig. 6: Change in R_s and R_d (ΔR_s and ΔR_d, respectively) of 100-nm-gate HEMTs. induced by bias and temperature stress. $\Delta R_d/\Delta R_s$ is plotted as a function of the recess length (L_{side}). Smaller L_{side} causes damage that is more localized in the drain side. This suggests that the principal cause of ΔR_d becomes weaker with increasing L_{side}, or, at least, ΔR_d is less influenced by L_{side}.

Hydrogen degradation of InP HEMTs and GaAs PHEMTs

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Hydrogen degradation in III-V field-effect transistors is a serious reliability concern. Hydrogen exposure of III-V FETs can occur when hydrogen outgases from packaging material and becomes trapped inside hermetically sealed modules. Over time, hydrogen leads to changes in the device characteristics which can ultimately cause parametric module failures. While this reliability problem has been documented in GaAs MESFETs and PHEMTs and InP HEMTs, its detailed physical origin has proven elusive. This paper will summarize the results of systematic experiments recently carried out at MIT towards understanding this problem and the physical mechanisms that have emerged [1-4].

Our work in the last few years has been based on InP HEMTs that were fabricated at MIT (L_G=0.7-10 μm), as well as on state-of-the-art InP HEMTs and GaAs PHEMTs from industry (L_G=0.1 μm). The use of MIT hardware allowed us to study a wide range of devices and test structures with different geometries. This proved key in the identification of the responsible mechanisms. The industrial devices have been studied as a test of the validity and portability of our conclusions.

Our experiments involve three major phases: N_2 burn-in, H_2 exposure, and N_2 recovery. N_2 burn-in is carried out at a higher temperature (230 °C) than H_2 exposure or N_2 recovery and for a time that is sufficient to exhaust any shift in the device characteristics due to purely thermal effects. H_2 exposure and N_2 recovery are carried out for long periods of time at 200 °C. We used forming-gas as H_2 source. H_2 exposure and N_2 recovery were performed in a temperature-controlled wafer probe station equipped with a sealed chamber. This allows for *in-situ* device measurements. We monitored device figures of merit characteristic of the intrinsic (low-field threshold voltage, V_T), and extrinsic portions of the device (off-state breakdown voltage, BV_{dg}). Devices with different gate lengths and gate orientations were studied. The result of a typical experimental run is shown in Fig. 1.

Our experiments on InP HEMTs fabricated at MIT have allowed us to identify three different physical effects associated with H_2 exposure. They are summarized in Fig. 2. First, H_2 is catalyzed by Pt in the Ti/Pt/Au gate stack and atomic H reacts with Ti to form TiH. This introduces compressive stress in the gate and tensile stress in the heterostructure underneath. Through the piezoelectric effect, an L_G-dependent shift in V_T and all the figures of merit associated with the intrinsic device takes place. This mechanism is found to be largely reversible. Second, H ions appear to diffuse into the intrinsic portion of the device also producing a small shift in V_T that is independent of L_G. This is also reversible. Third, in the recessed region of the extrinsic portion of the device next to the gate, hydrogen modifies the surface stoichiometry of the exposed InAlAs surface. This results in a reduction of the sheet carrier concentration underneath and a modification of device figures of merit associated with its extrinsic portion, such as BV_{dg}.

We have verified the existence of these mechanisms through independent experiments. TiH formation in the gate stack has been confirmed through AES. Compressive stress in H_2-exposed Ti/Pt films was verified through in-situ radius-of-curvature measurements (Fig. 3). Partial cycling of V_T was observed in bias-dependent H_2 exposure experiments. Changes in the native oxide of a H_2 exposed InAlAs surface have been detected through XPS. A reduction in the sheet carrier concentration of recessed heterostructures has been measured through the Hall effect.

Our experiments on state-of-the-art industrial InP HEMTs and GaAs PHEMTs with L_G=0.1 μm reveal a behavior largely consistent with the above results. There is strong evidence of stress-related phenomena in the time evolution of V_T during H_2 exposure (Fig. 4) and N_2 recovery. However, the *sign* of ΔV_T is contrary to that of the MIT devices. While in our [011]-oriented devices V_T always shifts negative (Fig. 1), in industrial GaAs PHEMTs and InP HEMTs of the same orientation, V_T shifts positive.

We are investigating the origin of this apparent contradiction by carrying out two-dimensional simulations of stress in HEMT structures using Abaqus. This is followed by a computation of the 2D piezoelectric charge distribution across the heterostructure and a solution of the resulting 2D electrostatic problem in MATLAB. Preliminary results for the 2D piezoelectric charge distribution in InP HEMTs for three different gate lengths are shown in Fig. 5. L_G is found to play a key role. In long devices, V_T appears to shift negative due to the polarization sheet charge that appears at the channel/insulator and channel/buffer interfaces as a result of the different polarization constants of these layers. In short devices, a prominent piezoelectric charge distribution in the volume of the intrinsic device shifts V_T positive. Depending on L_G, either one of these two competing processes might get to dominate with contrary implications to the sign of ΔV_T.

[1] R. R. Blanchard et al., IEDM'98, p. 231. [2] R. R. Blanchard et al., IEEE Electron Dev. Lett. 20, 393 (1999). [3] R. R. Blanchard et al., EMC'99. [4] R. R. Blanchard and J. A. del Alamo. IPRM'2000.

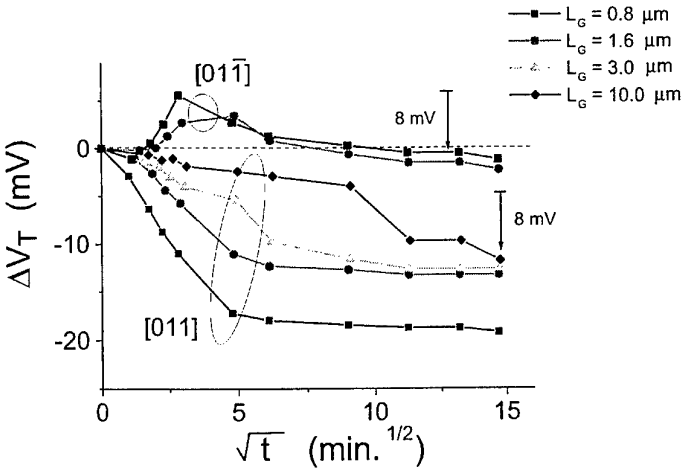

Fig. 1: ΔV_T vs. time under H_2 exposure at 200 °C for MIT's InP HEMTs. The 8 mV rigid shift, regardless of L_G and orientation, is evidence of penetration of H^+ into the heterostructure.

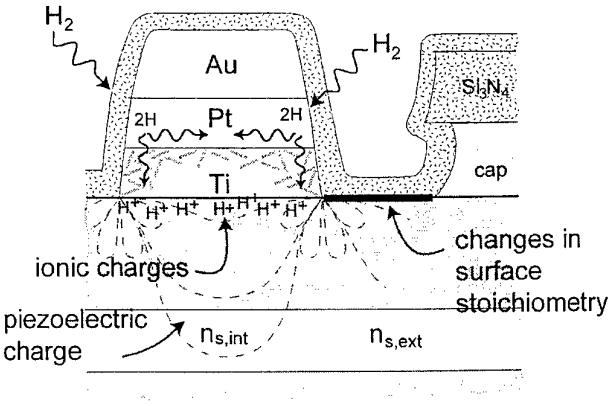

Fig. 2: Sketch depicting dominant H_2 effects in InP HEMTs.

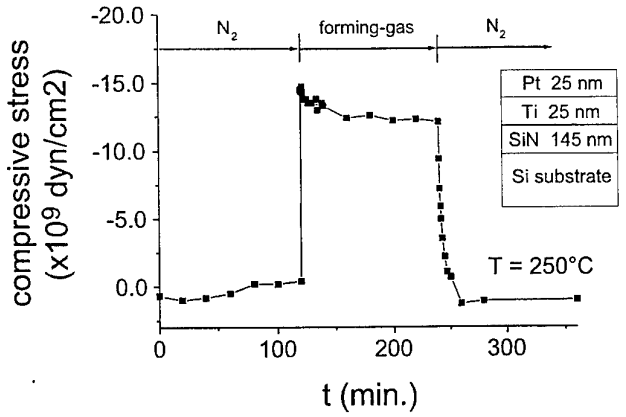

Fig. 3: In-situ stress measurement of a Ti/Pt bilayer under H_2 exposure and N_2 annealing.

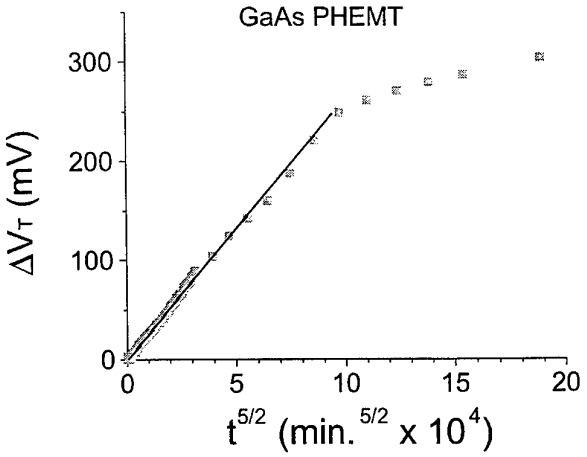

Fig. 4: ΔV_T for 0.1 μm GaAs PHEMT under forming gas exposure at 200 °C. The $t^{5/2}$ dependence of ΔV_T is characteristic of stress buildup due to formation of 2D platelets (presumably of TiH_x).

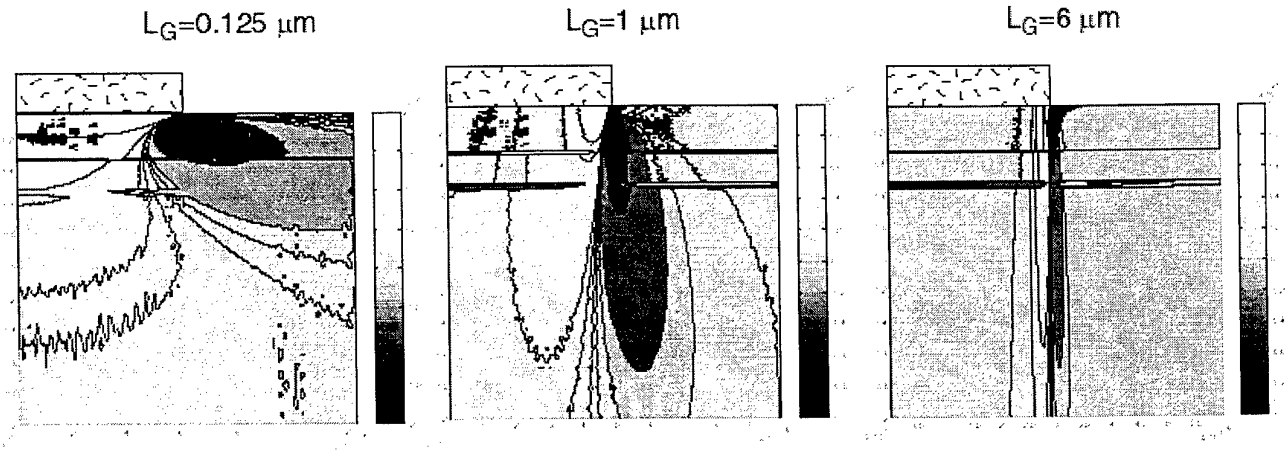

Fig. 5: 2D piezoelectric charge distribution in three double-heterostructure InP HEMTs with different L_G. Only half of the device is simulated. A sheet of charge appears at the channel/insulator and channel/buffer interface. The volume charge distribution is a strong function of L_G.

InGaP Channel FET with High Breakdown Voltage

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Power amplifiers with high output power are required for use in the base stations of wireless communications systems. Usually, high output power is obtained by increasing the total gate width of the field effect transistors (FETs), and output power around 150 W has been achieved [1-3]. However, a large gate width causes a decrease in the input and output impedances, resulting in an increase in the loss of matching circuits. Higher operating voltages are, therefore, required for further increasing output power.

The operating voltages of FETs are limited by both on-state and off-state breakdown voltages. On-state breakdown voltage (BV_{on}) is mainly limited by impact ionization in a channel region. Employment of a wide gap material is, therefore, effective for enhancing BV_{on}. Off-state breakdown voltage (BV_{off}) is determined by gate-to-drain breakdown voltage (BV_{gd}). A high BV_{off} is expected by employing wide-gap channel and barrier layers. We developed an InGaP channel FET structure [4] suitable for high voltage operation, which can be fabricated by using the conventional GaAs-based FET process.

A cross section of our new FET is shown in Fig. 1. We used epitaxial layers consisting of an $Al_{0.3}Ga_{0.7}As$ buffer layer, a Si-doped InGaP channel layer (150 nm, 1.5e17 cm^{-3}), an $Al_{0.3}Ga_{0.7}As$ barrier layer, and a GaAs cap layer. The bandgap energy of $In_{0.5}Ga_{0.5}P$ is about 1.9 eV, which is about 0.5 eV higher than that of GaAs. An increase in breakdown voltage is, therefore, expected. Furthermore, we also optimized a buffer layer to achieve high voltage operation.

Fig. 2 shows the band diagrams of some FETs previously reported. In conventional GaAs channel FETs, shown in Fig. 2 (a), a narrow-gap GaAs channel results in a low BV_{on}. The band-gap of the channel layer must be wide to reduce impact ionization and, hence, to obtain a high BV_{on}. In InGaP MESFETs [5], shown in Fig. 2 (b), an InGaP channel was employed and a high BV_{gd} was attained. In this FET, however, electrons also exist in a narrow-gap layer below the InGaP layer because a GaAs buffer layer was employed. Impact ionization occurring here, results in low BV_{on}. It means that a buffer layer is also important for obtaining a high BV_{on}. In our InGaP channel FETs, we used an $Al_{0.3}Ga_{0.7}As$ buffer layer to avoid the accumulation of electrons in the narrow-gap layer. Therefore, the bandgap is wide throughout the channel region, as shown in Fig. 2 (c) and a high BV_{on} can be expected. In addition, we inserted an $Al_{0.3}Ga_{0.7}As$ barrier layer between the gate electrode and channel layer to increase the BV_{gd}.

InGaP channel FETs can be fabricated using the conventional processes for fabricating GaAs-based FETs. Ohmic electrodes were formed on n^+-ohmic regions formed by Si ion implantation and activation annealing. Source-to-gate and gate-to-drain spacings were 1 μm and 2 μm, respectively, which are equivalent to those in conventional GaAs channel FETs. The gate length was 1.1 μm.

The I_{ds}-V_{ds} characteristics of the InGaP channel FET is shown in Fig. 3. BV_{on} (@ V_{gs}=0 V) exceeds 40 V. BV_{gd}, defined as $-V_{gd}$ at I_{gd}= -0.5 mA/mm, was about 55 V. Such high breakdown voltages are the result of the optimized AlGaAs/InGaP/AlGaAs structure. We also made on-wafer load-pull measurements to ensure the capability of large signal operation at a high operating voltage. The InGaP channel FETs were not destroyed even at V_{ds}=40 V. We confirmed, therefore, that the InGaP channel FETs have the expected high breakdown voltages and are suitable for high voltage operation.

Next, impact ionization was characterized by gate current measurements as proposed by Hui *et al.* [6]. Fig. 4 shows the relationship between $|I_{gs}/I_{ds}|$ and $1/(V_{ds}-V_{sat})$, where V_{sat} is the saturation voltage. When all holes generated by impact ionization flow into the gate electrode and this hole current dominates the gate current, $|I_{gs}/I_{ds}|$ corresponds to the product of impact ionization rate (α_n) and the effective length of the high-field region (L_{eff}). (V_{ds}-V_{sat}) is the product of the electric field (E) and L_{eff}. GaAs MESFET [6] and AlGaN/GaN HFET [7] data is also shown in Fig.4. The InGaP channel FET is positioned between GaAs and GaN-based FET from the viewpoint of impact ionization, as expected from band-gap energy.

In summary, we fabricated high-breakdown-voltage FETs with an InGaP channel layer and optimized AlGaAs buffer and barrier layers, which can be fabricated by conventional processes used for GaAs FETs. Due to a reduction in impact ionization, an extremely high BV_{on} (@V_{gs}=0 V) of over 40 V was achieved. A BV_{gd} of 55 V was also obtained, thereby achieving high-voltage large-signal operation at 40 V.

References

[1] I. Takenaka, H. Takahashi, K. Asano, K. Ishikura, J. Morikawa, K. Sato, I. Takano, K. Hasegawa, K. Tokunaga, F. Emori, and M. Kuzuhara, Technical Digest 1998 GaAs IC Symposium, 81 (1998).

[2] K. Ishikura, K. Asano, H. Takahashi, I. Takenaka, J. Morikawa, M. Kuzuhara, 1998 Asia-Pacific Microwave Conference Digest, 1255 (1998).

[3] Y. Tateno, H. Takahashi, T. Igarashi, and J. Fukaya, 1999 IEEE MTT-S Digest, 1087 (1999).

[4] N. Hara, Y. Nakasha, T. Kikkawa, H. Takahashi, K. Joshin, Y. Watanabe, H. Tanaka, and M. Takikawa, Technical Digest 1998 IEDM, 63 (1998).

[5] Yo-Sheng Lin and Shey-Shi Lu, IEEE Electron Device Lett. **17**, 452 (1996).

[6] K. Hui, C. Hu, P. George, and P. K. Ko, IEEE Electron Devices Lett. **11**, 113 (1990).

[7] N. Dyakonova, A. Dickens, M. S. Shur, and R. Gaska, Electron. Lett. **34**, 1699 (1998).

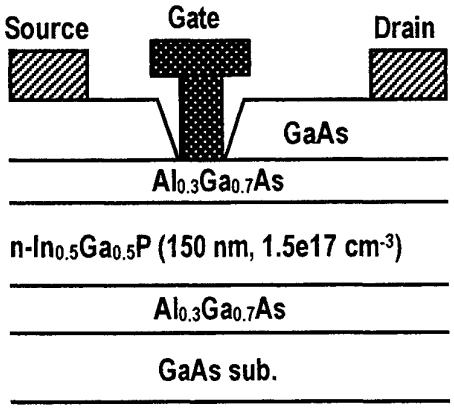

Fig. 1 Cross section of a newly developed InGaP channel FETs.

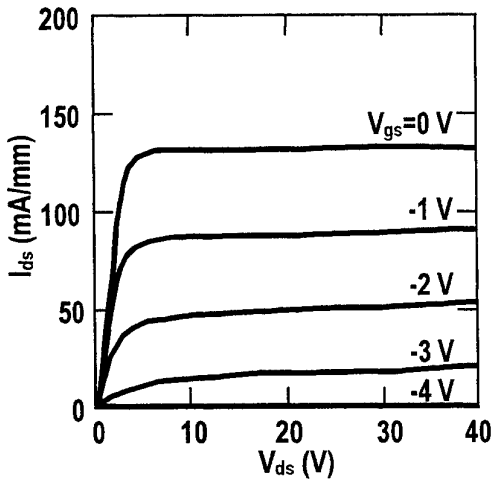

Fig. 3 I_{ds}-V_{ds} characteristics of our InGaP channel FET with a gate length of 1.1 μm. V_{gs} was changed from -4 V to 0 V in 1 V steps.

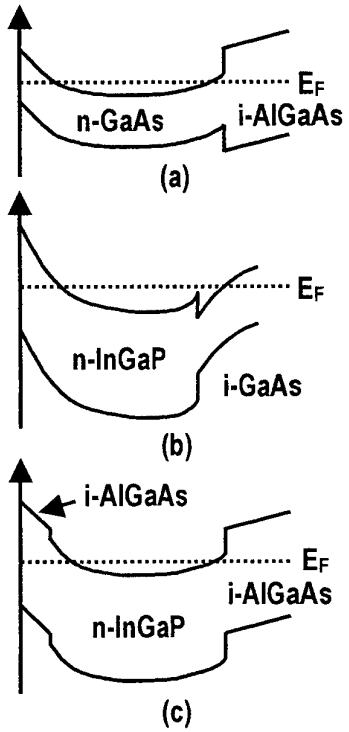

Fig. 2 Band diagrams under the gate electrode of (a) conventional GaAs MESFET, (b) InGaP channel MESFET with a GaAs buffer layer [5], and (c) our InGaP channel FET with AlGaAs buffer and barrier layers.

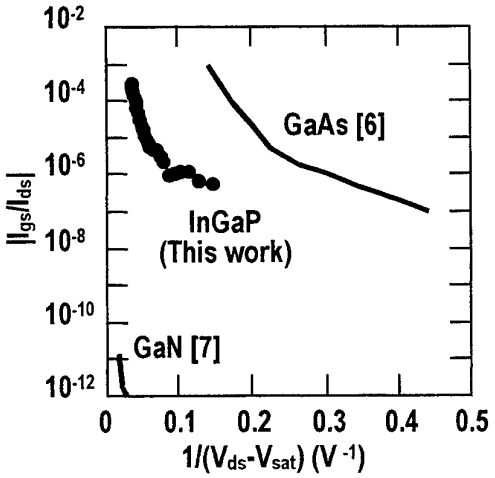

Fig. 4 Relationship between $|I_{gs}/I_{ds}|$ and $1/(V_{ds}-V_{sat})$ of the InGaP channel FET. Data of GaAs MESFET [6] and AlGaN/GaN HFET [7] are also shown.

III-V MOSFET Using Ga_2O_3/Gd_2O_3 As The Gate Oxide

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The III-V based metal-oxide-semiconductor field effect transistors (MOSFETs) potentially have great advantages over Si-based MOSFETs for high-speed low power logic integrated circuits (ICs) and monolithic microwave integrated circuits (MMICs), due to the five times higher electron mobility in GaAs and the availability of semi-insulating GaAs substrates. In contrast to GaAs metal-semiconductor FETs (MESFETs) and high electron mobility transistors (HEMTs), which exhibit small forward gate voltages limited by the Schottky barrier heights, GaAs MOSFETs feature a much larger logic swing which gives a greater flexibility for digital IC designs.

Previously, extensive efforts have been devoted to the realization of a feasible III-V based MOSFET. However, the drain current drift and hysteresis hinder the success of GaAs MOSFETs due to the difficulty in fabricating an insulating film with insignificant bulk trapped charges and a low interfacial density of states on GaAs. Recently, we have demonstrated enhancement-mode *p*- and *n*-channel GaAs MOSFETs with inversion and a midgap interfacial density of states in the mid 10^{10} $cm^{-2}eV^{-1}$, using a molecular beam epitaxy (MBE) grown $Ga_2O_3(Gd_2O_3)$ as the gate dielectric. In this talk, we present enhancement-mode n- and p-channel, depletion-mode GaAs MOSFETs as well as enhancement-mode InGaAs MOSFETs using $Ga_2O_3(Gd_2O_3)$ as the gate oxide.

Sample fabrication was performed in a multi-chamber ultra high vacuum (UHV) system, which includes a solid source III-V compound semiconductor molecular beam epitaxy (MBE) chamber, an arsenic-free UHV oxide deposition chamber, and UHV wafer transfer modules. The growth sequence starts with the growth of epilayers. The wafers were then transferred *in-situ* under UHV to the second chamber for the deposition of $Ga_2O_3(Gd_2O_3)$ films. Once the growth was completed, the wafers were removed from the UHV system for subsequent studies and/or processing.

The InGaAs based n-channel enhancement-mode MOSFETs showed excellent performances such as an extrinsic transconductance of 190 mS/mm, and an effective mobility of 470 cm^2/Vs. The drain I-V characteristic is illustrated in Figure 1. The devices did not exhibit hysteresis. The depletion-mode GaAs MOSFET has also exhibited negligible drain current drift and hysteresis. The short-circuit current-gain cutoff frequency (f_T) and the maximum oscillation frequency (f_{max}) were measured by biasing the devices at V_{ds} = 2 V and V_{gs} = -1.5 V. The f_T = 17 GHz and the f_{max} = 60 GHz for a 0.8-μm gate-length device were determined by extrapolating the short-circuit current-gain (H_{21}) and the maximum stable gain (MSG) curves, respectively, using –20 dB/decade slopes. Large gate width power devices were fabricated with this technology and the performance of a 1 μm × 2.4 mm device reveals that the GaAs depletion-mode MOSFET is a promising candidate for use in microwave power amplifiers. Figure 2 and 3 show the SEM of the device and a power measurement of the device.

The first inversion-channel enhancement mode GaAs MOSFET of both n- and p-configurations was demonstrated in 1996. The gate oxide was deposited after the 800 °C activation for the source-drain implantation. The roughness between the oxide/semiconductor degraded the device performance. Recently, he device performances of inversion-channel MOSFET's were greatly improved with a modified processing approach by depositing the oxide before the implantation. The drain currents of an inversion n-channel GaAs MOSFET have now been increased from 50 μA to 3 mA for devices with 1 μm gate length. Figure 4 shows typical drain current versus drain voltage characteristics of such a device. The maximum drain current density and the extrinsic transconductance of 30 mA/mm and 4 mS/mm, respectively, were achieved.

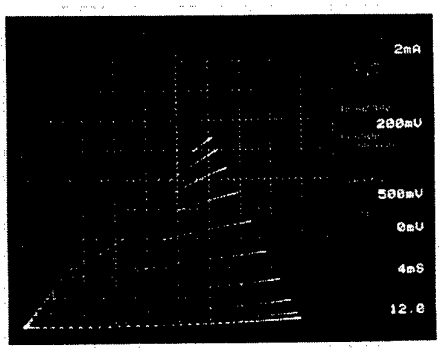

Fig. 1. Drain I-V of an enhancement-mode n-channel InGaAs MOSFET.

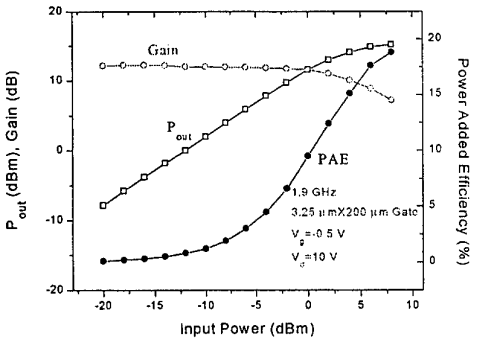

Fig. 3. Power characteristics of a depletion-mode GaAs MOSFET device.

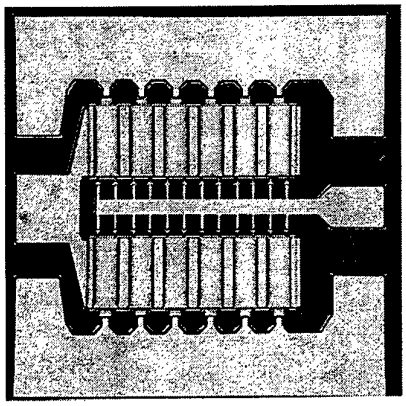

Fig. 2. SEM of a depletion-mode n-channel GaAs power transistor.

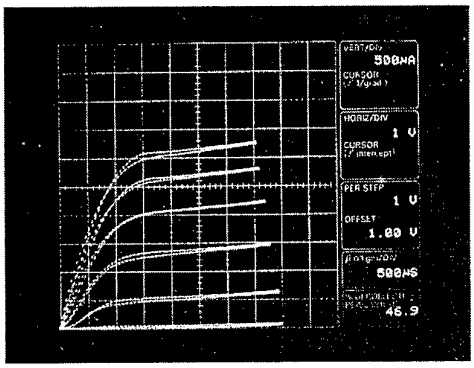

Fig. 4. Drain I-V characteristics of a enhancement-mode n-channel GaAs MOSFET.

An InGaP/GaAs Composite Channel FET for High Power Device Applications

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InGaP has been thought to be attractive material for high power device applications because of the wider band gap (1.9 eV) and lower impact ionization coefficient than those of GaAs. Some papers have reported high breakdown-voltage FETs with an InGaP channel. The obtained results showed high breakdown voltage, however, the transconductance (g_m) is low due to the low electron mobility of InGaP(~1000 cm/v・sec).

We propose an InGaP/GaAs composite channel (C-C) FET in order to obtain both a high g_m and a high breakdown voltage for high power device applications.

The cross section of InGaP/GaAs C-C FET is shown in Fig. 1. An i-GaAs buffer, i-AlGaAs buffer layer, 750 Å n-InGaP sub-channel, 100Å i-GaAs channel, and i-AlGaAs cap layer were successively grown by low pressure OMVPE. An i-AlGaAs buffer was used for the electron confinement in the InGaP. We also fabricated the InGaP single channel (without GaAs channel) FET at the same time for comparison.

The pricipal operation of InGaP/GaAs C-C FET is based on the difference in the electrron distributions under the source and drain sides of the gates. At the source side where the electric field is low, the two-dimensional electron gas located in GaAs with high electron mobility. On the other side, at the drain side where the electric field is high, the electron transferred to the InGaP with high breakdown field. A higher mobility is useful to reduce the source parasitic resistance resulting in an increase of the g_m. A higher breakdown field is useful to increase the breakdown voltage of FET.

In addition, the Γ valley of InGaP has lower energy level than the L valley of GaAs, so that the hot electron in GaAs transfers to the Γ valley in InGaP as opposed to the L valley in GaAs (see Fig.2). The electron velocity of the Γ valley of InGaP is higher than that of the L valley of GaAs. It is expected that this will improve the high field electron transport property of InGaP/GaAs composite channel.

The low field electron mobility of the single and the composite channel structure are 1000 cm/v・sec and 1800 cm/v・sec, respectively. The fabricated devices have the ion-implanted source/drain region, and 1.2 μm ×20 μm gates with a planar structure.

The I-V characteristics of the InGaP single channel FET and the InGaP/GaAs C-C FET are shown in Fig. 3 (a) and (b), respectively. The Vg-Ids, g_m characteristics of the single channel FET and the C-C FET are shown in Fig. 4 (a) and (b), respectively.

The on-state breakdown voltage (BV_{ds}) of both FETs is almost the same and is larger than 25 V. The two-terminal breakdown voltage (BV_{bd}) of both FETs is also almost the same, larger than 35 V. On the other hand, the g_m of the C-C FET is higher than that of the single channel FET. The Ids of the C-C FET is higher than that of the single channel FET. The higher g_m and larger Ids of the C-C FET are due to the high electron mobility in GaAs. The high breakdown voltage of the C-C FET is evidence that the electrons at the drain side locate in the InGaP.

The summary of the DC characteristics of both FETs is shown in Table 1.

The RF and power characteristics will be presented.

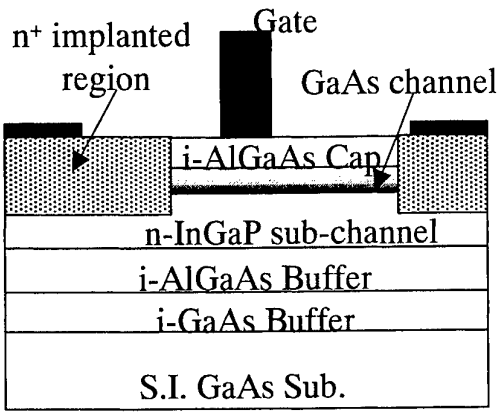

Fig. 1 Cross section of the composite channel FET

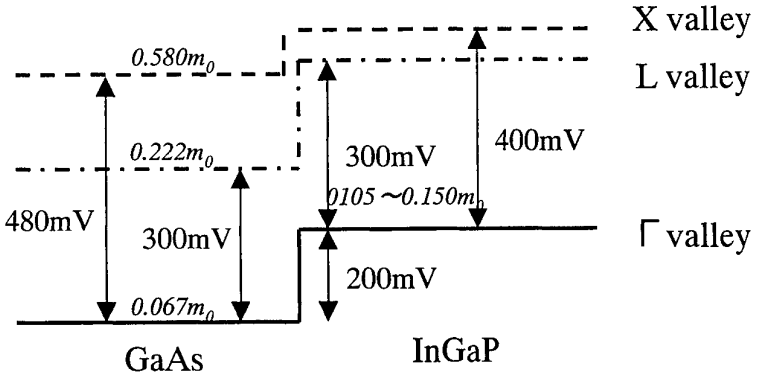

Fig. 2 Conduction band energy diagram of InGaP/GaAs hetero-structure

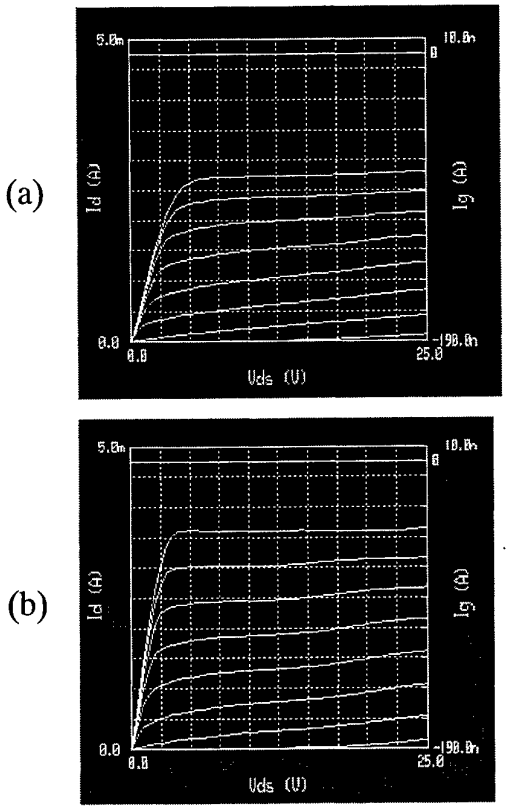

Fig. 3 I-V characteristics of the InGaP FET (a) InGaP/GaAs composite channel FET (b)
Vgstart = 0.6 V, Vgstep = -0.6 V

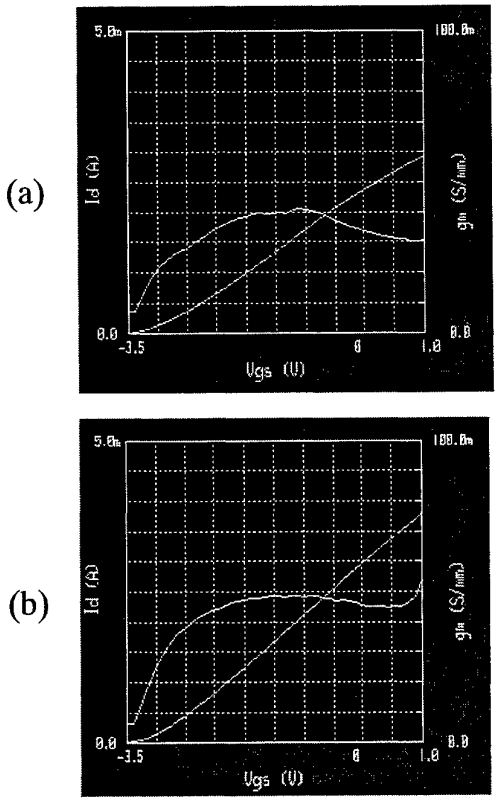

Fig. 4 Vg - Ids, g_m characteristics of the InGaP FET (a) InGaP/GaAs composite channel FET (b)
Vds = 6.0 V

Table 1. Summary of DC characteristics of InGaP FET and InGaP/GaAs composite channel FET

Lg = 1.2 μ m
Wg=20 μ m

	Vth (V)	Idmax (mA)	Ron (Ω)	g_{mmax} (mS/mm)	BVbd (V)	BVds (V)
InGaP	-3.49	2.90	29.6	44	-37	> 25
InGaP/GaAs	-3.47	3.75	14.4	56	-35	>25

Device Linearity and Gate Voltage Swing Improvement by $Al_{0.3}Ga_{0.7}As/In_{0.15}Ga_{0.85}As$ Double Doped-channel Design

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Abstract

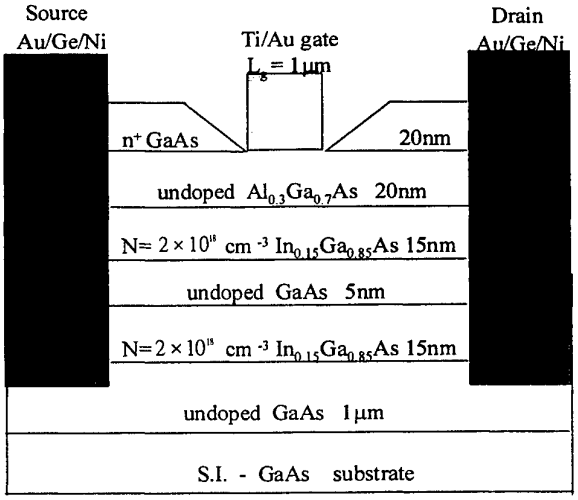
Double doped-channel AlGaAs/InGaAs FET's (D-DCFETs) have been proposed, fabricated, and compared with the conventional doped-channel FET's (DCFETs). The double doped-channel design increases the total sheet charge density and doubles the effective channel width without the critical thickness limitation in the InGaAs channel, which enhances the device characteristics. We also compare the devices linearity with $Al_{0.3}Ga_{0.7}As/In_{0.2}Ga_{0.8}As$ HEMTs, which have better carrier confinement than $In_{0.15}Ga_{0.85}As$ channel. These advantages suggest that D-DCFETs is more suitable for linearity, and high RF power devices applications.

The AlGaAs/InGaAa/GaAs D-DCFETs heterostructures were grown in a Riber-32p molecular beam epitaxy (MBE) system on (100)-oriented semi-insulating GaAs substrates. Two 15 nm thick pseudomorphic $In_{0.15}Ga_{0.85}As$ doped channels were grown on top of an 1.0 μm undoped GaAs buffer layer, and a 5 nm undoped GaAs layer is inserted in these two InGaAs channels. Finally, a 20 nm undoped $Al_{0.3}Ga_{0.7}As$ layer, and a 20 nm n^+-GaAs capping layer were grown to improve the Schottky and ohmic contacts, respectively. For comparison, the layers for conventional single doped-channel and HEMTs with 3 nm spacer were grown.

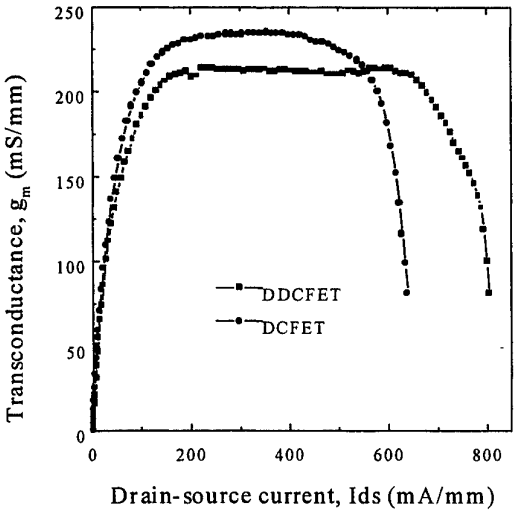
The Schottky turn-on and (breakdown) voltages of D-DCFETs, DCFETs and HEMTs are 1.1 V (-23V), 1.0V (-23 V) and 0.7 V (-13V), respectively. The g_m and threshold voltage (gate voltage swing for 90% g_m) are 214 mS/mm, –2.5 V (2.75 V) for D-DCFETs, 235 mS/mm, -1.5 V (1.75 V) for DCFETs, and 300 mS/mm, –0.5 V (0.8V) for HEMTs. No significant gate leakage was found in D-DCFETs even for a gate bias voltage of 1V, and the output conductance can be as low as 1 mS/mm for a 660 mA/mm channel current. A dramatic increase in channel current as well as good current linearity in a wide range of gate voltage can be found in D-DCFETs; the maximum drain current is 815 mA/mm for D-DCFETs, 650 mA/mm for DCFETs, and 350 mA/mm for HEMTs. If we express the I_{ds}-V_{gs} curves by a 6th order polynomial form to describe the output characteristics as: $I_{ds}=A_0+A_1V_{gs}+A_2V_{gs}^2+A_3V_{gs}^3+A_4V_{gs}^4+A_5V_{gs}^5+A_6V_{gs}^6$, where An's are independent variables which can determine the linearity associated with I_{ds}-V_{gs} transfer characteristics, we find that the values An's/A_1 for D-DCFETs were much smaller than those for DCFETs and HEMTs. Therefore, a higher linearity power performances can be expected for the D-DCFETs by suppressing the 3rd(or higher)-order inter-modulation.

Microwave on-wafer S-parameters for 1.0 mm-long gate devices were measured by an HP-8510 network analyzer. An f_t and (f_{max}) of 20 GHz (41 GHz) for D-DCFETs, 22 GHz (33 GHz) for DCFETs were obtained at V_{ds}=2.5 V, respectively. For DCFETs, a decrease of both f_T and f_{max} started to occur at I_{ds} > 400 mA/mm. However, no significant performance reduction was observed for D-DCFETs till I_{ds} = 600mA/mm. Microwave power performances were characterized at V_{ds} = 2.5V under a 1.9 GHz operation for gate dimension of 1× 150 μm devices. Linear power gain was 19 dB for D-DCFETs and 17.4 dB for DCFETs. The maximum output power and PAE were 16.6 dBm (305 mW/mm) and 51.5 % for D-DCFETs, and 14.5 dBm (188 mW/mm) and 45 % for DCFETs, respectively.

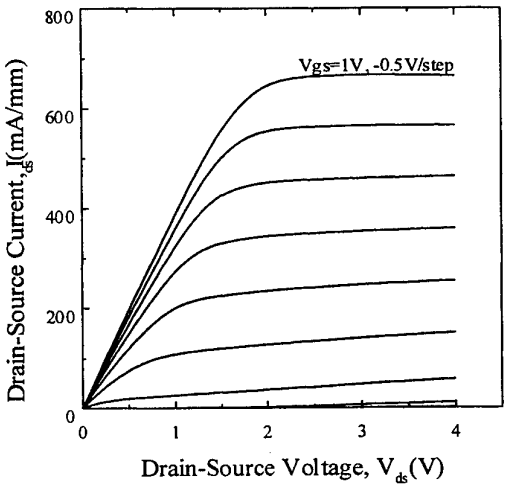
In conclusion, pseudomorphic $Al_{0.3}Ga_{0.7}As/In_{0.15}Ga_{0.85}As$ HFETs with a double doped-channel design have been fabricated. Based on this design, a higher sheet charge density is obtained resulting in a linearity improvement. The D-DCFETs demonstrates a wider input signal swing together with a higher current driving capability and better power performances, making this device to be a more suitable for microwave power device application.



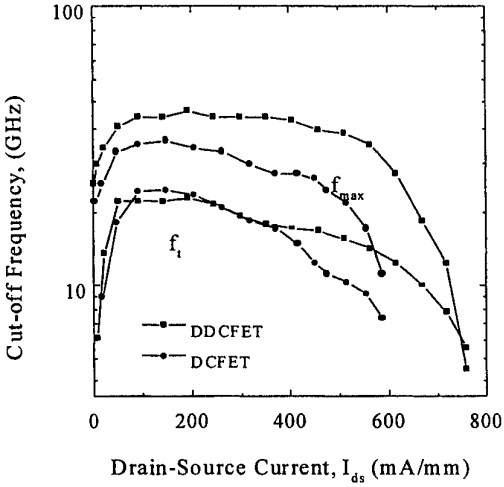
Device cross-section of AlGaAs/InGaAs D-DCEFTs



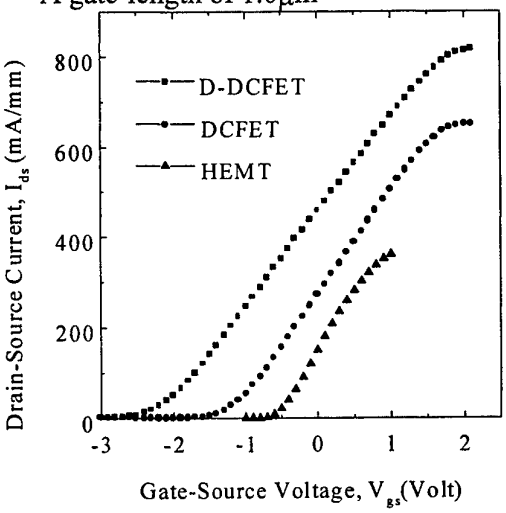
I_{ds}-g_m characteristics for D-DCFETs and DCFETs



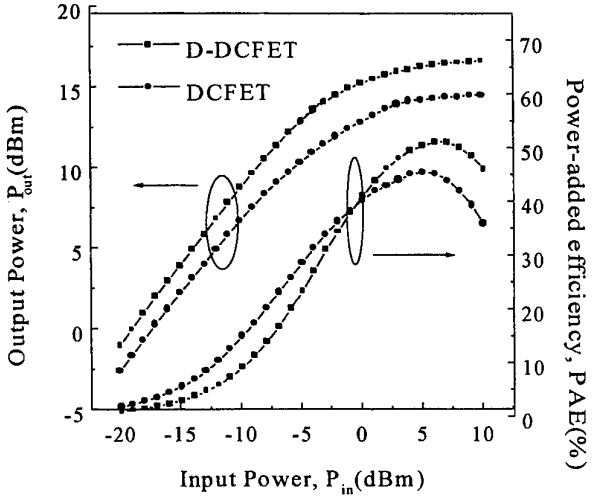
Device I_{ds}-V_{ds} characteristics of D-DCFETs wirh A gate-length of 1.0μm



I_{ds} dependence of f_T and f_{max} for D-DCFETs and DCFETs



I_{ds}-V_{gs} characteristics of D-DCFETs, DCFETs, and HEMTs



Output power and PAE performances of DCFETs and D-DCFETs (gate width: 150μm)

An	A0	A1	A2/A1	A3/A1	A4/A1	A5/A1	A6/A1
D-DCFETs	460	211.8	-0.037	0.004	0.011	-0.009	-0.002
DCFETs	265	236.9	0.106	0.111	-0.014	0.035	0.004
HEMTs	150	301.4	-0.068	-0.601	0.415	0.199	-0.247

Comparisons of harmonic distortion factors between D-DCFETs, DCFETs, and HEMTs

$In_{0.49}Ga_{0.51}P/In_{0.15}Ga_{0.85}As$ doped-channel HFETs with low parasitic resistances by inserting a Siδ-doped layer

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Abstract

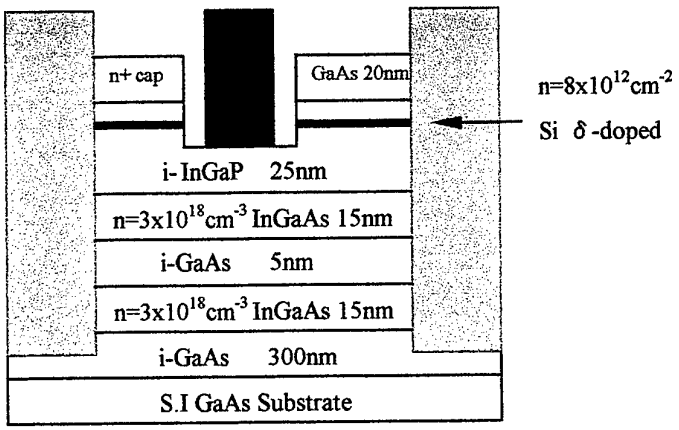
A high-barrier gate on InGaP/InGaAs doped-channel FET(DCFETs) provides a high-current density , high-gate-to-drain breakdown voltage and a better linear operation over a wide-gate bias range. However, doped-channel devices are often limited by large parasitic source and drain resistances associated with a 20nm undoped InGaP layer beneath the gate metal. In this study, we inserted a Siδ-doped layer inside this high bandgap undoped InGaP layer to reduce parasitic resistances and to enhance device DC and RF power performances.

Based on this modified InGaP/InGaAs DCFETs(M-DCFETs), the sheet charge density was $5.7\times10^{12}cm^{-2}$ with a Hall mobility of $1250cm^2/V\text{-}s$,and the device knee voltage (V_k), defined as the V_{ds} value where the Ids equals 100mA/mm at V_{gs} =0.5 V ,is 0.29V comparing with conventional DCFETs this value is 0.41V. A low knee voltage will be beneficial for device power performance, especially operated at low bias conditions. M-DCFETs provides a higher current density and larger transconductance than those in DCFETs. The peak g_m and saturation current are 230mS/mm and 880mA/mm for M-DCFETs and 204mS/mm ,810mA/mm for DCFETs.

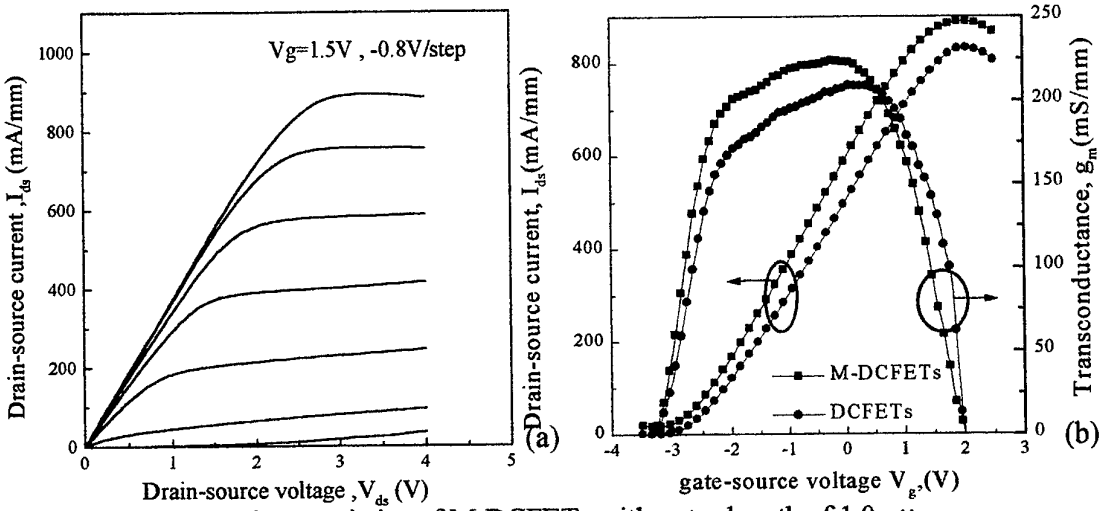
Based on the S-parameter measurements, we obtained an f_T=13GHz and an f_{MAX}=30GHz for M-DCFETs and 11GHz, 28GHz for DCFETs at V_{ds}=2.5V. By extracting the small-signal equivalent circuit model, we obtained a Rs of 4.7Ω and a Rd of 7.2Ω for M-DCFETs, and these values are 6.8Ω and 9.3Ω for DCEFTs without this Si δ -doped layer. The linear power gains of 15.8dB for M-DCFETs and 14.4dB for DCFETs, were observed at 1.8GHz. Maximum output power was 15.7 dBm(248mW/mm) for M-DCFETs and 14.7dBm(197mW/mm) for DCFETs, and associated maximum PAE was 24% for M-DCFETs, and 19 % for DCFETs respectively. A much better power performance of M-DCFETs, compared with DCFETs is attributed to the lower source and drain resistances of M-DCFETs.

M-DCFETs provides lower parasitic resistances and a higher current density by using a Si δ -doped layer in undoped InGaP layer, resulting in a high output power and a better PAE. This technology is promising for microwave power device application.

[Ref] Kraus,S.,Hei β ,H., Xu,D., M.Sexl, G.Bohm, G.Trankle and G.Weimann" InGaAS/InAlAs HEMTs with extremely low source and drain resistances" *Electron. Lett.*, 1996,vol. 32, no. 17, pp. 1619-1620

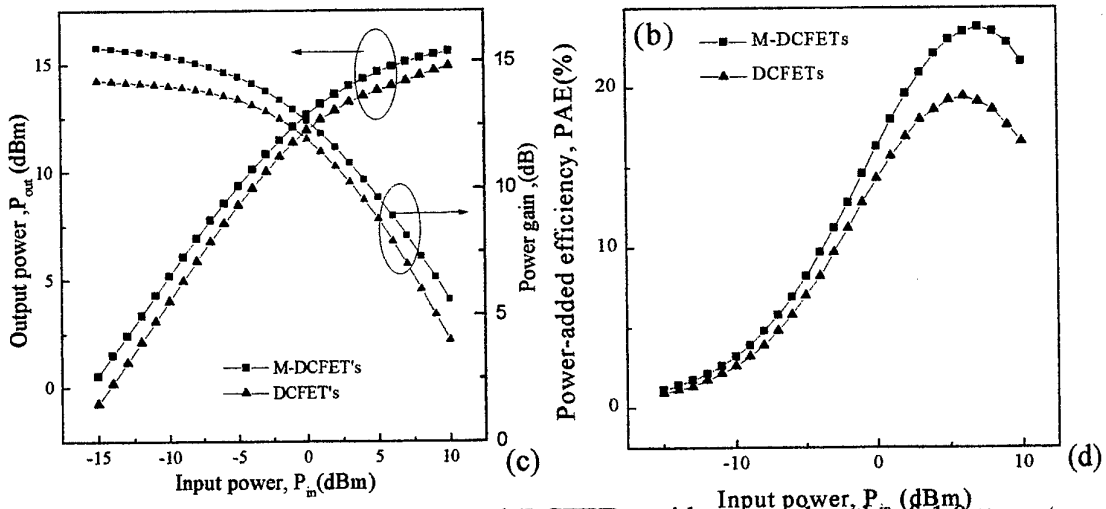


Device cross-section of $In_{0.49}Ga_{0.51}P/In_{0.15}Ga_{0.85}As$ doped channel FETs with planar Si δ – doped layer(M-DCFETs).



(a) I_{ds}-V_{ds} characteristics of M-DCFETs with gate -length of 1.0 μ m

(b) Transconductance and I_{ds}-V_{gs} characteristics of M-DCFETs and DCFETs at V_{ds}=3V.



Power performance of M-DCFETs and DCFETs ,with a gate length of 1.0 μ m at 1.8GHz (c)output power and power gain versus input power, and (d)power added efficiency versus input power.

Low-Frequency Noise Characteristics of AlGaAs/$In_xGa_{1-x}As$ Pseudomorphic HEMTs

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It is very important to study low-frequency (LF) noise in the HEMTs, because the LF noise limits the performance of ultrawide-bandwidth circuits and nonlinear circuits that have noise upconversion. In this report, we have extensively studied the LF noise characteristics of AlGaAs /$In_xGa_{1-x}As$ pseudomorphic HEMTs with a large InAs mole fraction [1].

The schematic cross-section of the measured HEMTs is shown in Fig.1. A thick (~1μm) $In_{x/2}Ga_{1-x/2}As$ buffer layer was grown on a GaAs substrate. This buffer layer is so thick that the strain in the buffer layers is fully relaxed. Thus the buffer layer acts as a substrate with an intermediate lattice constant for the pseudomorphic HEMTs, permitting us to use an $In_xGa_{1-x}As$ channel with a large InAs mole fraction. In the present study, the HEMTs with x = 0,0.2,0.4 and 0.5 were measured.

Fig.2 shows the gate current (I_G) noise spectra at room temperature. A Lorentz-type spectrum was superimposed on the 1/f characteristics at about 10 kHz for the devices with x = 0 and 0.2, suggesting the existence of deep level which causes generation-recombination (G-R) noise. Fig.3 shows the drain current (I_D) noise spectra for the samples biased at saturation regions (V_{DS} = 1.5 V) at room temperature. G-R noise component is observed for all kinds of devices.

The temperature dependence of the noise spectra was studied to obtain the activation energies of traps that cause the G-R noises. The Arrhenius plots ($T^2\tau$ vs 1/T) are shown in Fig.4. Here, $1/\tau$ is a corner frequency at which Lorentz spectrum appears. The results of I_G noise are shown by closed symbols and those of I_D noise by open symbols. Dotted lines are the fitting lines. All data are plotted close to each other with activation energies of 0.32 ~ 0.39 eV, suggesting that the G-R noise is caused by the same origin. Deep levels in AlGaAs obtained by DLTS [2] are also shown in Fig.4 by solid and dashed lines. Present results are near the level of 0.42 eV which corresponds to the DX center in n-AlGaAs. The observed G-R noises are presumably caused by the DX center.

The reason why I_G noise spectra of the devices with x = 0.4 and 0.5 follow an almost pure 1/f trend can be understood if we take into account the large lattice mismatch which leads to the inferior crystal quality. In this case, deep levels with different time constant τ will be induced. If the distribution function of the deep level is proportional to $1/\tau$, the spectral noise density varies as 1/f [3]. Fig.5 shows I_G noise power density, which increased with increasing InAs mole fraction at lower frequencies. This supports the above discussion.

LF noise at small drain bias was found to be strongly dependent on gate voltage, which is in good agreement with a model proposed by Peransin [4].

[1]T. Mizutani et al., Solid-State Electronics, vol.41, no.10, 1469(1997)
[2]K. Hikosaka et al., Inst. Phys. Conf. Ser., no.63, 233(1981)
[3]A. Van Der Ziel, Physica XVI, no.4, 359, April(1950)
[4]J-M. Peransin et al., IEEE Trans. Electron Devices, vol.37, no.10, 2250, October(1990)

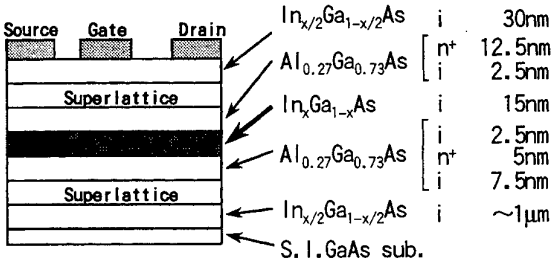

Fig.1. Schemastic cross-section of the AlGaAs/$In_xGa_{1-x}As$ pseudomorphic HEMT.

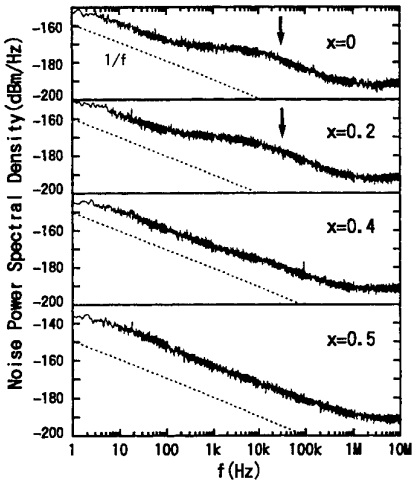

Fig.2. The gate current noise spectra at room temperature; V_{GS}=0.8V.

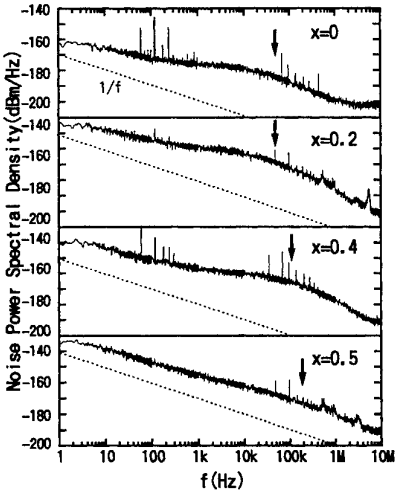

Fig.3. The drain current noise spectra; T=room temperature ,V_{DS}=1.5V, V_{GS}=0V for x=0, 0.2, 0.4 and 0.5V for x=0.5.

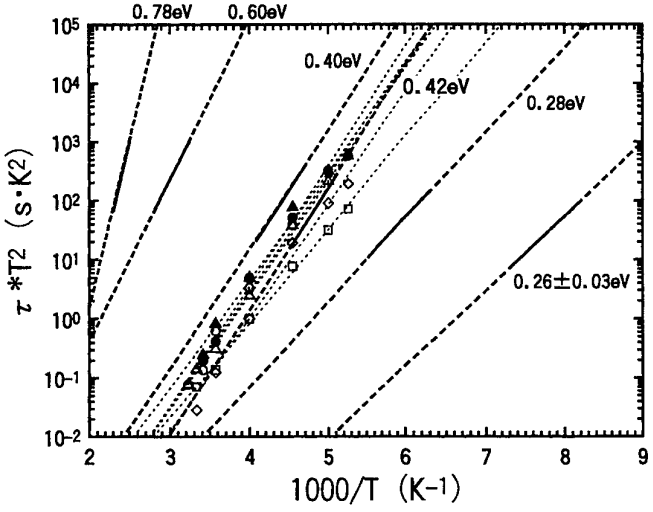

Fig.4. Arrhenius plots.
Closed and open symbols are the results of gate and drain current, respectively. Dotted lines are the fitting lines. Solid and dashed lines are deep levels in AlGaAs [2].

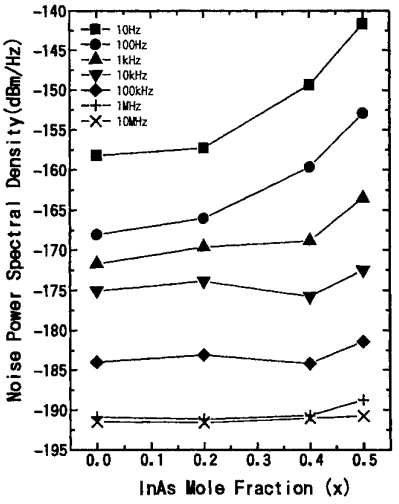

Fig.5. Noise power spectral density as a function of InAs mole fraction.

0.15-μm T-shaped gate MODFETs using BCB as low-k spacer

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Abstract

We report 0.15-μm T-shaped gate MODFETs using BCB (Benzocyclobutene) (k=2.7) as low-k spacer dielectric material. More than 20 GHz increase of f_{max} was obtained comparing to conventional SiO_2 spacer [1] by reducing the fringing gate capacitance. The BCB film is deposited by plasma CVD technique at 100℃ and is patterned by lift-off technique. The technique provides conformal 0.15-μm gate length by using phase shift i-line lithography, which has high throughput.

The T-shaped gates are widely used to achieve short gate length without increasing the gate resistance. In such structure, gate capacitance is major limiting factor of high frequency performance. The gate capacitance consists of gate-channel capacitance C_{gi} and fringing capacitance C_{gf} of T-gates. While the gate-channel capacitance C_{gi} can be reduced by shorting the gate length, the fringing capacitance C_{gf} is determined by the thickness and dielectric constant of spacer material. C_{gf} becomes relatively high as narrowing the gate length. We developed a novel gate process with BCB low-k spacer for this purpose.

Figure 1 shows the process steps of T-shaped gate technique with BCB. (1) A 0.2-μm dummy gate was defined by i-line pattern-edge line method. Then the dummy gate was trimmed in O_2 plasma to reduce the pattern width to 0.15-μm. (2) BCB film was deposited by plasma CVD technique at 100 ℃. Conventional spin-coated BCB needs to bake over 200 ℃. However, the dummy gate pattern is changed the shapes at such temperature. Therefore it is necessary to deposit BCB below 150 ℃. (3) The BCB was lifted off and a inverted 0.15-μm pattern was formed. (4) Ti/Au and NiAuGe were used for gate and ohmic electrodes, respectively. Figure 2 shows a cross-sectional SEM micrograph of BCB film (a) before and (b) after lift-off. The obtained dielectric constant was k=2.7 with the leak current of 4.7×10^{-5} A/cm^2 at 40 V for the BCB thickness of 110 nm.

AlGaAs/InGaAs MODFETs has been fabricated by using above T-shaped gate process. Figure 3 shows schematic cross-section of the fabricated MODFET. Figure 4 shows obtained DC performance of the FET with the L_g and W_g of 0.15 μm and 150 μm, respectively. The device showed the extrinsic transconductance gm_max of 600 mS/mm. A current-gain-cutoff frequency f_T and a maximum frequency of oscillation f_{max} as high as 80 GHz and 176 GHz were obtained, respectively as shown in figure 5. Figure 6 shows the relationship between the BCB thickness of dielectric spacer layer and f_T or f_{max}. The extracted C_{gs} with BCB spacer was 0.134 pF as compared with 0.181 pF with SiO_2 spacer. The C_{gd} with BCB spacer was 0.046 pF and the C_{gd} with SiO_2 spacer was 0.052 pF, respectively. More than 20 GHz increase in f_{max} was obtained by reducing the gate capacitance as compared conventional SiO_2 film.

[1] H. Takenaka, D. Ueda, IEEE Trans. Electron Devices, vol. 43, pp238-244, 1996.

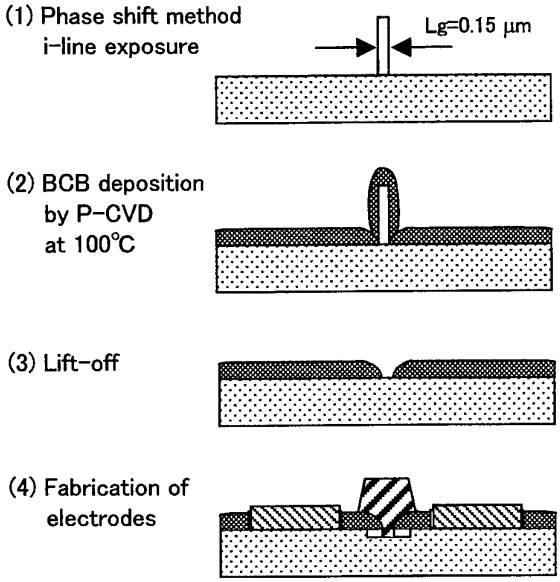

Fig. 1 Process steps of MODFETs with BCB

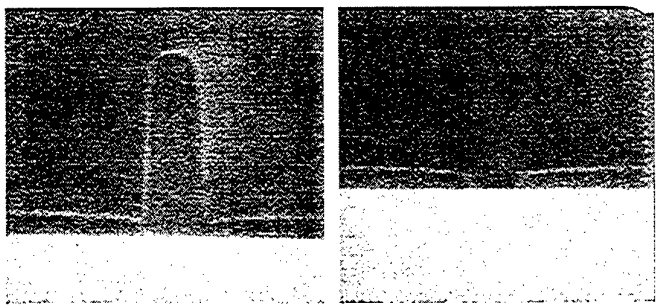

Fig. 2 SEM micrographs of patterned BCB film
(a) Before lift-off (b) After Lift-off

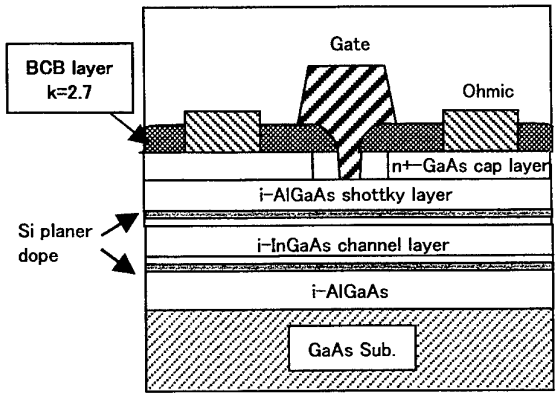

Fig. 3 Schematic cross-section of fabricated MODFET

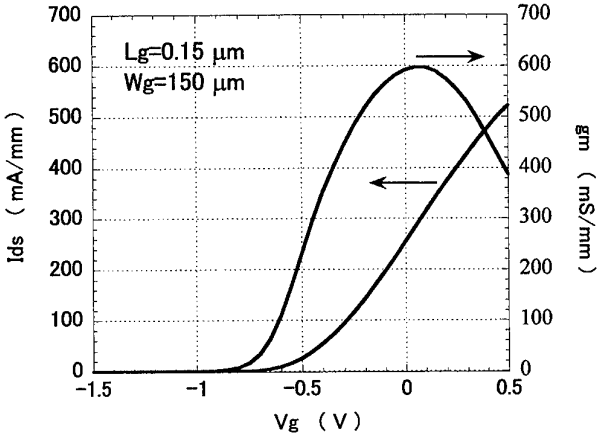

Fig. 4 Vg-Ids characteristic

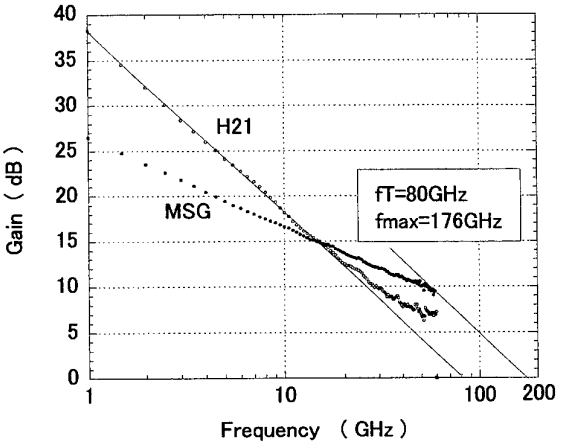

Fig. 5 RF characteristic

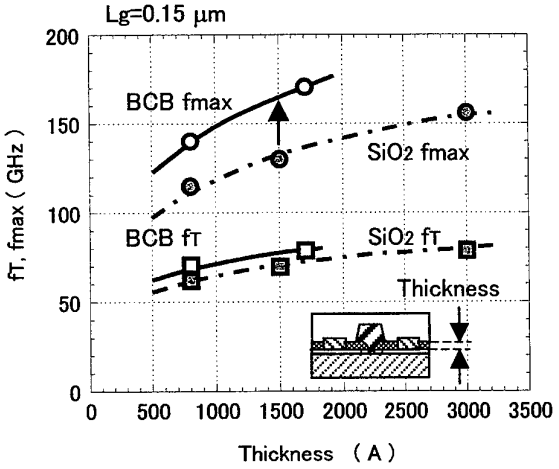

Fig. 6 BCB Thickness vs. ft, fmax

High RF Performance of 50-nm-Gate Lattice-Matched InAlAs/InGaAs HEMTs

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InP-based InAlAs/InGaAs high electron mobility transistors (HEMTs) show ultra-high RF performance because of their greater sheet electron density and faster equivalent average electron velocity, compared with AlGaAs/GaAs HEMTs. Nguyen *et al.* [1] reported cutoff frequency f_T of 340 GHz for 50-nm-gate pseudomorphic HEMT that has an InGaAs channel layer with a 0.8 indium content. For lattice-matched HEMT ($In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$), Suemitsu *et al.* [2] reported f_T of 350 GHz for 30-nm-gate HEMT. In this paper, we are reporting excellent RF performance of 50-nm-gate InP-based lattice-matched HEMTs fabricated in a conventional process under low temperatures.

HEMT epitaxial layers were grown on semi-insulating (100) InP substrates by metalorganic chemical vapor deposition (MOCVD). The layers, from bottom to top, consist of a 300-nm InAlAs buffer, 20-nm InGaAs channel, 3-nm InAlAs spacer, Si-δ-doped sheet (5×10^{12} cm^{-2}), 20-nm InAlAs and 40-nm Si-doped InGaAs cap (5×10^{18} cm^{-3}) layer. Since degradation of epitaxial structure during fabrication has a strong effect on DC and RF characteristics of HEMTs, all of the fabrication process described below was carried out under 300°C to prevent fluorine contamination and suppress possible diffusion of the Si-δ-doped sheet. Source and drain ohmic contacts were formed by alloyed AuGe/Ni/Au. The measured contact resistance was typically 0.07 Ω mm. T-shaped Ti/Pt/Au Schottky gates with a length of 50 nm and widths of 2 x 50 μm were fabricated using electron beam (EB) lithography and a standard lift-off technique within a source-drain spacing of 2 μm. Figure 1 shows both a schematic cross-section of the HEMT and a cross-sectional transmission electron microscope (TEM) image of a 50-nm-long T-shaped gate.

On-wafer DC and RF characteristics were measured at room temperature. Figure 2 shows the typical *I-V* characteristics of a 50-nm-gate HEMT. The device is well pinched off, and the maximum DC transconductance g_m of about 0.91 S/mm was achieved. S-parameters were measured in a frequency range from 0.25 to 50 GHz in 0.25 GHz steps. Figure 3 shows the frequency dependence of current gain $|h_{21}|^2$ of the 50-nm-gate HEMT. The parasitic capacitance caused by the probing pads was subtracted from the measured S-parameters. f_T of 362 GHz was obtained by the extrapolation of $|h_{21}|^2$ in a frequency range from 10 to 50 GHz, where the slope of least-squares fitting of $|h_{21}|^2$ is -20 dB/decade, as expected. This f_T is the highest value ever reported for any transistor. Figure 4 shows the L_g dependence of f_T of our HEMTs and that of HEMTs in previous works [2, 3]. Our 50-nm-gate HEMT has much higher f_T than those in previous works. To explain the remarkable enhancement of f_T in our HEMTs, we tried to analyze the transit time of electrons $\tau_{transit}$ by following a procedure similar to the method described in ref. [4]. Figure 5 shows the L_g dependence of $\tau_{transit}$ of our HEMTs. The transit time for the short channel device is expressed as

$$\tau_{transit} = (L_g + \Delta L) / v_s, \qquad (1)$$

where L_g is the gate metal length, $L_g + \Delta L$ is the effective gate length, and v_s is the saturation velocity of electrons. ΔL is considered to be resulting from side etching of the gate recess and expansion of the depletion layer toward the drain [3]. We obtained ΔL = 16 nm and $v_s = 2.6 \times 10^7$ cm/s by least-squares fitting in a range from 50 to 1000 nm, as expressed by the solid line in Fig. 5. Although determining L_g from a cross-sectional TEM image has some experimental errors, ΔL might be supposed to be in a range from 10 to 20 nm to reproduce experimental tendency. On the other hand, Enoki *et al.* obtained ΔL = 30 nm and $v_s = 2.7 \times 10^7$ cm/s [3], and Nguyen *et al.* obtained $v_s = 2.6 \times 10^7$ cm/s by a different procedure [1]. Despite slight differences in saturation velocity, the ΔL of our HEMTs is much shorter, resulting in higher f_T. The source of ΔL is the carrier depletion region between gate and drain caused by a high drain-to-gate voltage. The side-etched region of the gate recess, especially, causes the carrier depletion region to further expand. Since we paid a lot of attention on keeping the wafer temperature below 300°C during the whole fabrication process, a higher electron density in the gate recess region was able to be maintained by suppressing degradation of the epitaxial structure. Therefore, the shorter ΔL of our HEMTs might have resulted from the low-temperature fabrication process.

In summary, we fabricated 50-nm-gate lattice-matched InAlAs/InGaAs HEMTs using conventional EB and wet-chemical processes, and measured DC and RF characteristics at room temperature. We obtained an excellent cutoff frequency f_T of 362 GHz, which is the highest value ever reported for any transistor.

References

[1] L. D. Nguyen, A. S. Brown, M. A. Thompson, and L. M. Jelloian, IEEE Trans. Electron Devices **39**, 2007 (1992).
[2] T. Suemitsu, T. Ishii, H. Yokoyama, T. Enoki, Y. Ishii, and T. Tamamura, Jpn. J. Appl. Phys. **38**, L154 (1999).
[3] T. Enoki, M. Tomizawa, Y. Umeda, and Y. Ishii, Jpn. J. Appl. Phys. **33**, 798 (1994).
[4] T. Enoki, K. Arai, and Y. Ishii, IEEE Electron Device Lett. **11**, 502 (1990).

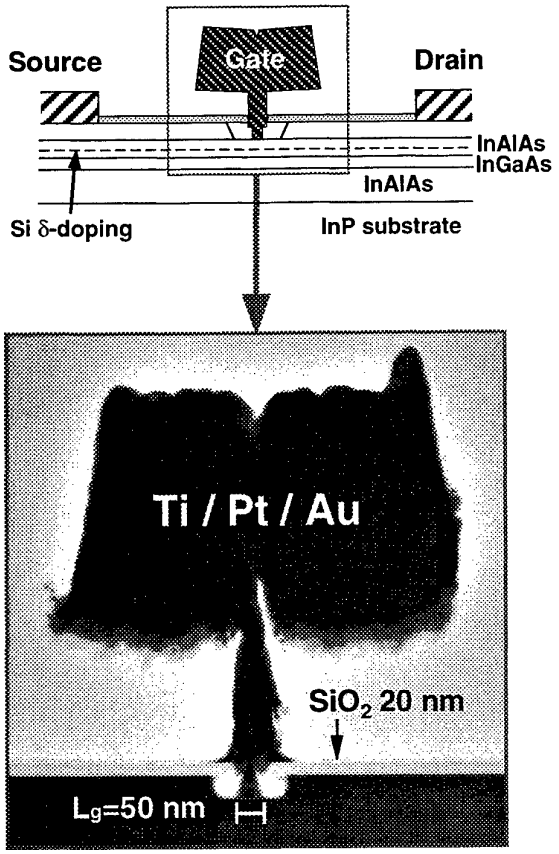

Fig. 1. Schematic cross-section of HEMT and cross-sectional TEM image of a 50-nm-long T-shaped gate.

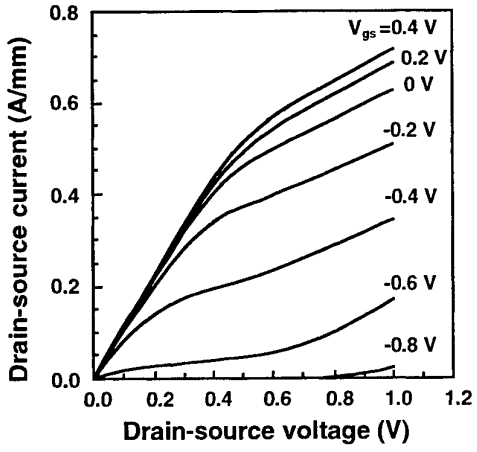

Fig. 2. *I-V* characteristics of 50-nm-gate HEMT. The gate-source voltage V_{gs} is decreased from 0.4 V (top) to -0.8 V (bottom) in -0.2 V steps.

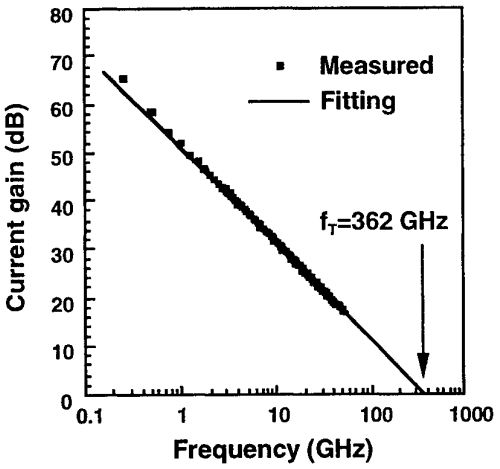

Fig. 3. Frequency dependence of current gain $|h_{21}|^2$ for 50-nm-gate HEMT. The drain-source voltage V_{ds} is 0.9 V, and gate-source voltage V_{gs} is -0.4 V. f_T is 362 GHz by the extrapolation of $|h_{21}|^2$ using least-squares fitting.

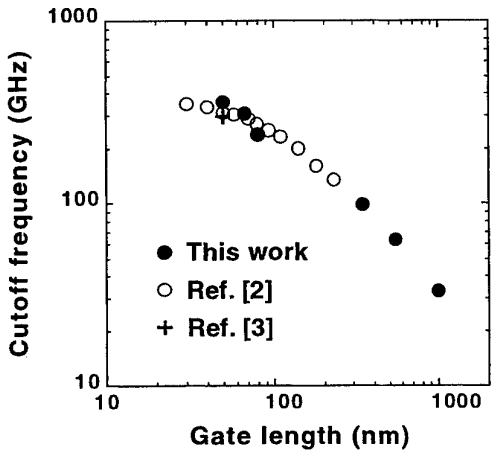

Fig. 4 Gate length L_g dependence of cutoff frequency f_T.

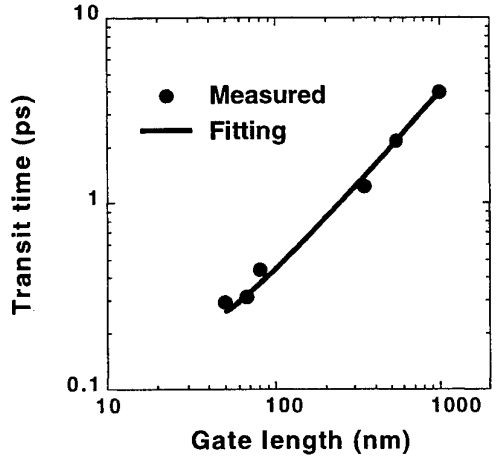

Fig. 5 Gate length L_g dependence of transit time of electrons $\tau_{transit}$. The solid line indicates the least-squares fitting result using ΔL = 16 nm and v_s = 2.6 x 10^7 cm/s in eq. (1).

Temperature Dependence of High-Frequency Performance of InAlAs/InGaAs HEMTs

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InAlAs/InGaAs HEMTs have attracted much attention due to their potential for high-speed and high-frequency circuit applications. Better performance is expected at cryogenic temperatures, however, there are few reports on the performance of InAlAs/InGaAs HEMTs at cryogenic temperature. In this report, the performance of $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ HEMTs were measured at various temperatures using a low-temperature on-wafer prober.

The InAlAs/InGaAs HEMT structure was grown by MBE and shown in Fig.1. Following the formation of the non-alloyed ohmic contacts and the deposition of SiO_2 passivation film with 50 nm thickness, T-shaped gate was fabricated by EB lithography and SF_6 RIE. The gate length and the source-drain spacing were 0.1 and 2.5 μm, respectively. The fullerene-incorporated nano-composite EB resist [1] was used for the gate pattern delineation to enhance dry-etching resistance.

The measured cutoff frequency (f_T) was shown in Fig. 2 as a function of the gate voltage. The highest cutoff frequency of 83 GHz was obtained at V_G = - 0.2 V and V_{DS} = 1.8 V at room temperature. Relatively low f_T is probably due to the large overlap capacitance of the T-shaped gate.

Fig. 3 shows the total delay time ($\tau = 1/2\pi f_T$) plotted as a function of the inverse of the drain current for various temperatures at V_{DS} = 1.8 V. The delay time decreased linearly with decreasing the inverse of the drain current. The linearly decreasing term in the figure is the channel charging time, which reaches zero at an infinite I_{DS}. Then the extrapolated intersects at $1/I_{DS} = 0$ is the sum of the intrinsic delay (L_G/v_{sat}) and the drain delay ($(R_S + R_D)C_{GD}$) [2]. The different intersects for the different temperatures show that the effective saturation velocities (v_{sat}) are dependent on the temperature. The effective saturation velocities are 1.6 x10^7 and 2.0 x10^7 cm/s at 300 and 50 K, respectively. Here it was assumed that the drain delay was 0.2 ps and the effective gate length was 0.15 μm considering the extension of the depletion layer at the source and drain end of the gate (50 nm). The saturation velocity showed 25% increase with decreasing the temperature from 300 to 50 K. According to Houston [3], the v_{sat} at very high fields is given as follows assuming that the average carrier energy is much larger than the optical phonon energy.

$$v_{sat}=2\{(2/3\pi)(\hbar\omega_{jj}/(2n_{jj}+1))/m^*\}^{1/2}, \qquad n_{jj}=1/\{\exp(\hbar\omega_{jj}/kT)-1\}$$

Here, $\hbar\omega_{jj}$ is the optical phonon energy and T is the lattice temperature.

The calculated v_{sat} for $\hbar\omega_{jj}$ = 36 meV is shown by a solid line in Fig. 4. The measured temperature dependence of v_{sat} shown by closed circles is similar to the calculated one, suggesting that the average carrier energy in the channel is very high.

High-frequency measurements of InAlAs/InGaAs HEMTs with 0.1-μm-long gate have been performed at temperatures ranging from 50 to 300 K. 25 % increase in saturation velocity was observed by changing the temperature from 300 to 50 K. It is shown that the temperature dependence of the effective saturation velocity is similar to that of the calculation at very high field.

[1] T. Ishii, H. Nozawa, and T. Tamamura, Appl. Phys. Lett., vol. 70, pp. 1110, 1997.
[2] T. Enoki et al., IEEE Electron Device Lett., vol. 11, p. 502, 1990.
[3] P. A. Houston and A. G. Evans, Solid-State Electronics, vol. 20, pp. 197, 1977.

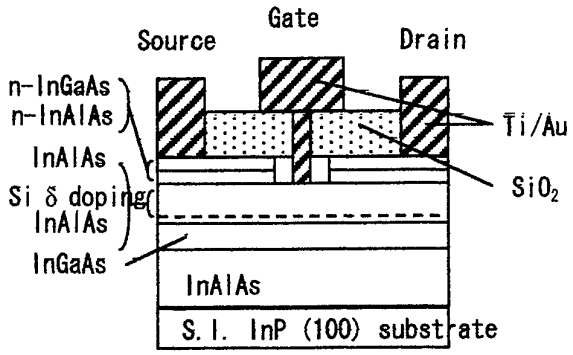

Fig. 1 Schematic cross-section of the fabricated InAlAs/InGaAs HEMTs.

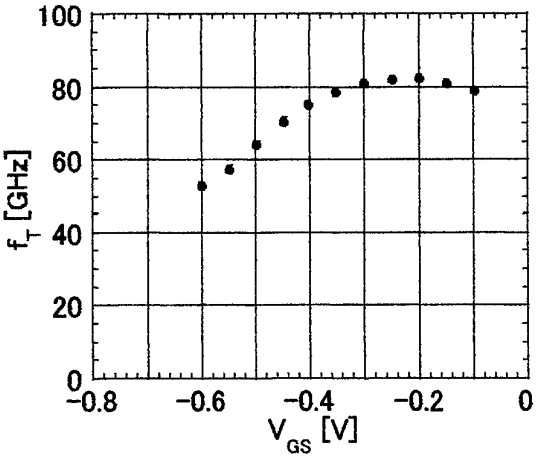

Fig. 2 Cutoff frequency as a function of the gate voltage at V_{DS} = 1.8 V and at room temperature.

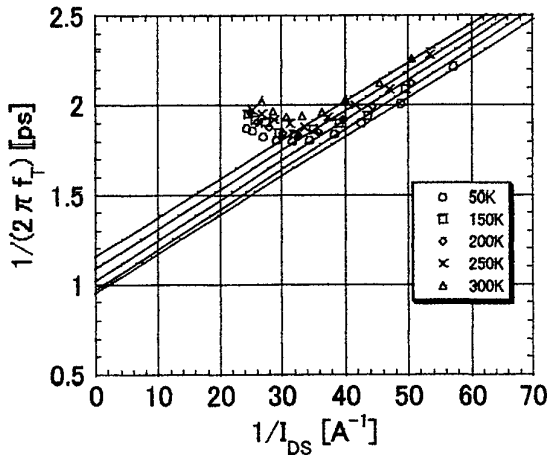

Fig. 3 Delay time as a function of the inverse of the drain current at V_{DS} =1.8 V.

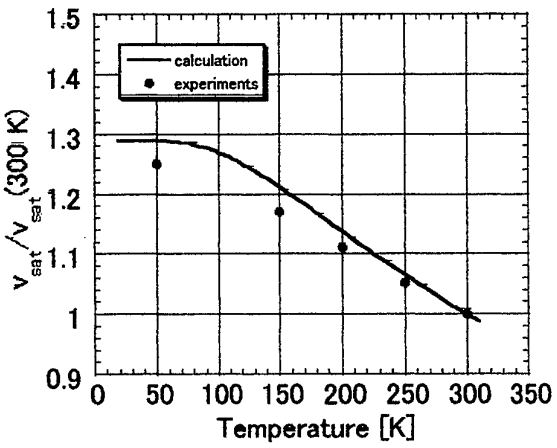

Fig. 4 Effective saturation velocity as a function of the inverse of the drain currrent at V_{DS} = 1.8 V.

Low Leakage, High Breakdown Voltage and High Transconductance Insulated Gate PHEMTs Utilizing Silicon Interface Control Layer

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The InP-based InGaAs/InAlAs pseudomorphic HEMT (PHEMT) is an important candidate for the key device in next generation wireless and optical communication networks due to its excellent high frequency performance. However, use of the Schottky gate structure with low and unstable barrier heights tends to cause problems such as large DC power consumption due to leakage currents, low breakdown voltages, poor power handling capability, poor reproducibility and poor reliability. Use of an insulated gate (IG) is one promising approach to solve these problems. However, it is very difficult to realize a good IG structure on III-V compound semiconductors due to strong Fermi level pinning at the insulator-semiconductor interfaces.

This paper reports on successful fabrication and DC and RF characterization of novel InGaAs/InAlAs IG-PHEMTs utilizing the silicon interface control layer (Si ICL) technology. It consists of insertion of an ultrathin MBE-grown Si layer between the compound semiconductor and a Si-based insulator so as to realize an ordered, coherent and pinning-free interface[1].

The plan-view and cross-sectional structures of the novel InP-based IG-PHEMT are shown in **Fig.1(a)** and **(b)**, respectively. The fabrication sequence is shown in **Fig.2**. The Hall mobility and sheet carrier density at 300 K were 7700 cm^2/Vs and $1.9x10^{12}$ cm^{-2}, respectively. After formation of ohmic electrodes and removing semiconductor surface oxides, 1 nm thick Si layer was formed by MBE and partial nitridation was done in ECR plasma CVD chamber to obtain ultrathin SiN_x/Si structure[2]. Then, 40 nm SiO_2 was deposited by plasma CVD. Cr/Au gate electrode was formed by conventional photolithograpy and lift-off process.

Use of the Si ICL had a dramatic effect. Without Si ICL, the IG-PHEMT showed poor gate control due to Fermi level pinning as shown in **Fig.3**. With Si ICL, the device showed a excellent gate control and complete channel pinch-off, as shown in **Fig.4**. The maximum transconductance, g_m, of 177mS/mm was achieved for gate length, L_G, of 1.6 μm. This is twenty times larger than the best g_m value of 7 mS/mm of the IG-PHEMT without Si ICL.

Gate leakage currents of the IG-PHEMT and a Schottky gate HEMT are compared in **Fig.5**. The reverse leakage current of the IG-PHEMT at V_G = -1 V was two orders of magnitude smaller than that of the Schottky gate device. The forward current were 5-7 orders of magnitude smaller, and remained below 1 nA even at V_G = +1 V, allowing positive gate bias operation. The gate-source and gate-drain breakdown voltages were as high as 38 V and 39 V, respectively.

In spite of a long gate length of L_G = 1.6 μm, the device showed respectable on-wafer RF characteristics as shown in **Fig.6**. f_T = 9 GHz and f_{max} = 38 GHz were obtained. A rather small f_T as compared with f_{max} seems to be due to a large gate capacitance C_G. Further improvement of both g_m and RF characteristics should be achieved by reducing the gate length with submicron gate and optimizing the gate insulator thickness.

[1] S. Kodama, S. Koyanagi, T. Hashizume and H. Hasegawa: Jpn. J. Appl. Phys. **34** (1995) 1143.
[2] T. Hashizume, K. Ikeya, M. Mutoh and H. Hasegawa: Appl. Surf. Sci. **123/124** (1998) 599.

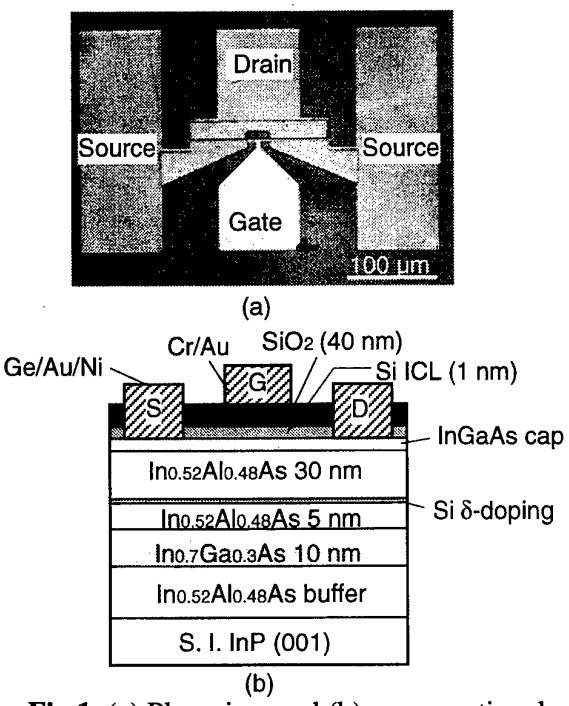

Fig.1. (a) Plan-view and (b) cross-sectional structures of the insulated gate PHEMT.

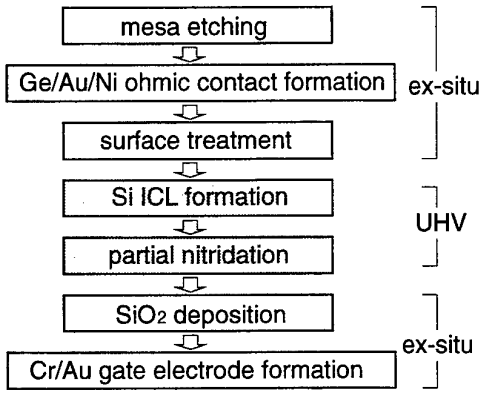

Fig.2. Device fabrication process.

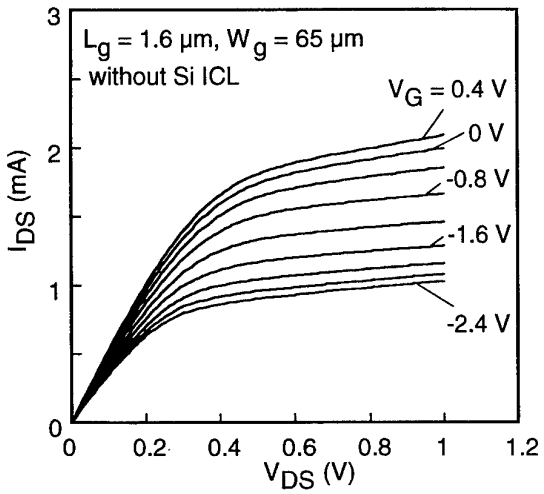

Fig.3. I_{DS}-V_{DS} characterisitics of IG-PHEMT withou;t Si ICL.

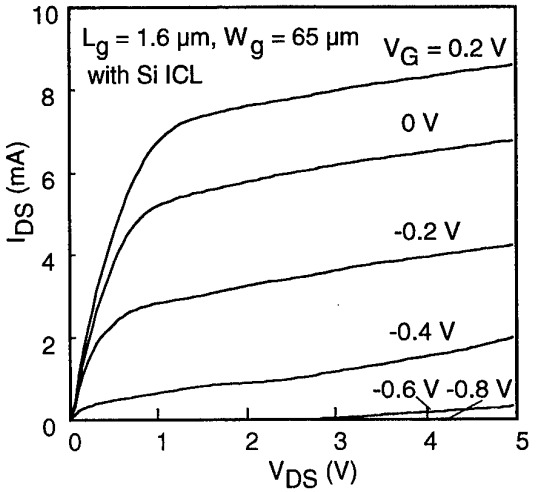

Fig.4. I_{DS}-V_{DS} characterisitics of IG-PHEMT with Si ICL.

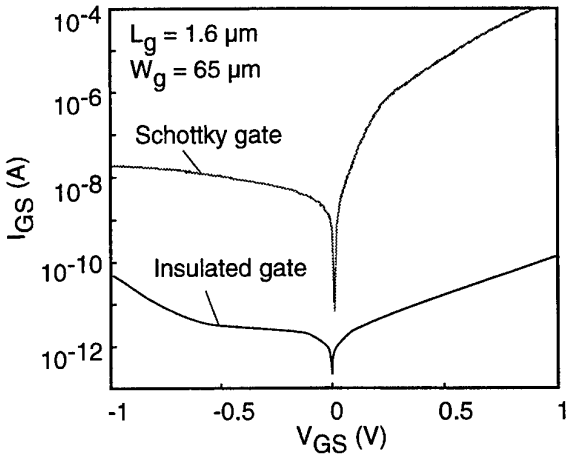

Fig.5. Gate leakage current characterisitics.

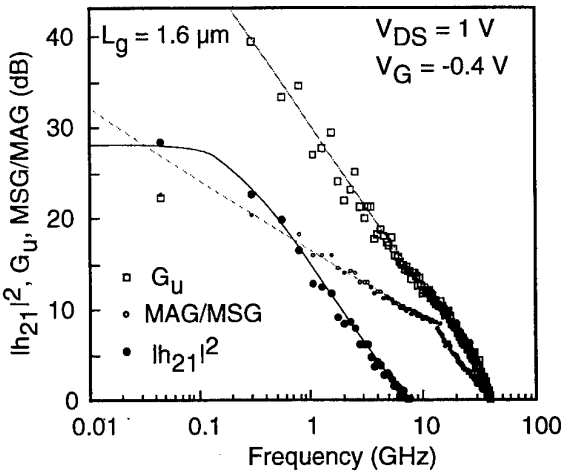

Fig.6. On-wafer RF characteristics.

Completely Oxide-Free Insulated Gate Structure Having Silicon Interface Control Layer for InP MISFETs

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InP is an extremely attractive channel material for high power microwave and milli-meter wave FETs due to its higher electron mobility, higher saturation drift velocity and higher thermal conductivity than those of GaAs. Since Schottky Barriers on InP show low and unstable barrier heights, an insulated gate (IG) structure is a favorable one. However, previous IG structures containing oxides were unstable primarily due to inevitable inclusion of In_2O_3 component. On the other hand, previous oxide-free IG structures showed poor gate control due to high density surface states causing Fermi level pinning.

In this paper, we describe a novel oxide-free and pinning-free IG structure of InP and its application to MISFETs. It utilizes an ultrathin SiN_x/Si layer produced by MBE growth of Si and its partial nitridation by an ECR N_2 plasma [1], as shown in **Fig. 1(a)** and **(b)**. The role of the resultant ultrathin Si interface control layer (Si ICL) is to terminate the surface bonds of InP and then the Si ICL itself is terminated by an ultrathin SiN_x layer formed by nitridation. In this structure, quantum states formed in the silicon surface quantum well is expected to behave like as interface states. However, these states are pushed away by quantum confinement effect if the thickness of Si ICL is reduced down to 5Å [1]. By further depositing a thicker Si_3N_4 layer, a novel IG structure is completed as shown in **Fig. 1(c)**.

In this study, Si layer was grown either directly on clean MBE InP surface (*in-situ* process), or on an air-exposed MBE InP surface after chemical etching and UHV thermal cleaning (*ex-situ* process).

The observed escape-angle dependence of the angle-resolved Si *2p* XPS spectra shown in **Fig. 2** indicated that ultrathin SiN_x/Si ICL (~6Å) structure was realized by the ECR nitridation. Electronic properties of InP surfaces before and after Si ICL formation was monitored *in-situ* in UHV by the UHV contactless C-V method [2], which allows an MIS assessment of the processed surfaces utilizing the UHV gap (200~400nm) as an insulator. *In-situ* process enhanced variation of the capacitance as shown in **Fig. 3**. **Figure 4** shows interface state density (Nss) distributions calculated from UHV C-V curves. These results clearly show that *in situ* passivation process is favorable, realizing a full swing of Fermi level almost over the entire bandgap of InP.

InP MISFETs without Si ICL showed almost no gate control. With Si ICL, the devices started to show respectable gate control as shown in **Fig. 5** for the *ex-situ* and the *in-situ* processes. The *in-situ* process improved I-V characteristics, and showed about three times enhancement of g_m value than that of the *ex-situ* processed device. The gate leakage current characteristics of the fabricated MISFET was compared with the electron beam (EB)-deposited Pt/InP Schottky diode, as shown in **Fig. 6**. It is clear that the gate leakage current of the MISFET was reduced about 1/100 to 1/1000 at reverse and forward biases, respectively. **Figure 7** shows the drain current drift characteristics of the fabricated MISFET with *in-situ* Si ICL process after applications of a gate voltage step of -1V. As seen, only an extremely small drain current drift of 1.9% was observed after 10^4 s operation. These results indicate that our Si ICL based passivation is very effective in realizing stable high power InP MISFET.

[1] H. Takahashi, T. Hashizume, H. Hasegawa, Jpn. J. Appl. Phys. **38** (1999) 1128.
[2] H. Takahashi, T. Yoshida, M. Mutoh, T. Sakai and H. Hasegawa, Solid State Electron. **43** (1999) 1561.

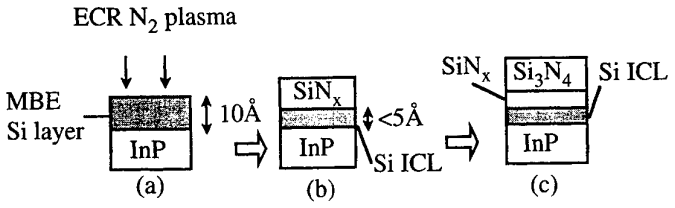

Fig. 1. A novel insulated gate structure.

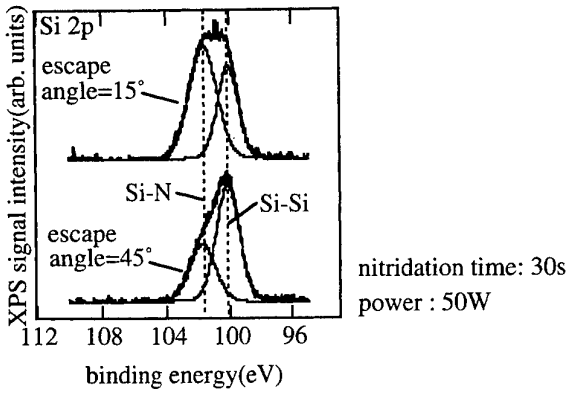

Fig.2. Si *2p* XPS core-level spectra obtained from the Si ICL/InP interface after nitridation of Si ICL by ECR N_2 plasma.

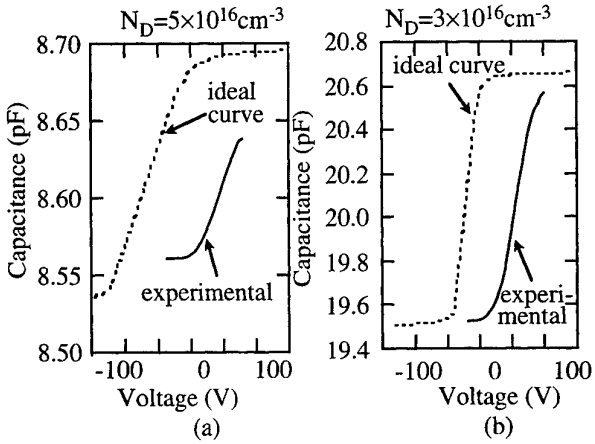

FIg. 3. UHV contactless C-V curves of InP surfaces after 30s nitridation of Si ICL: (a) *ex-situ* process and (b) *in-situ* process.

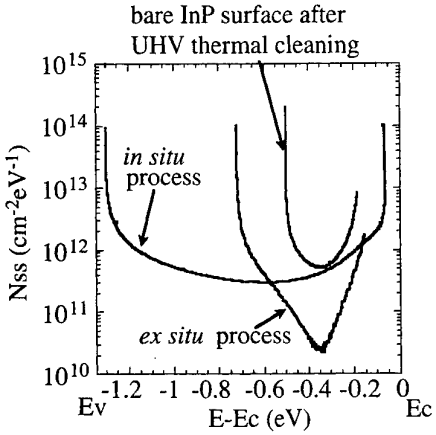

Fig. 4. Nss distributions after nitridation of Si ICL calculated from the UHV C-V curves.

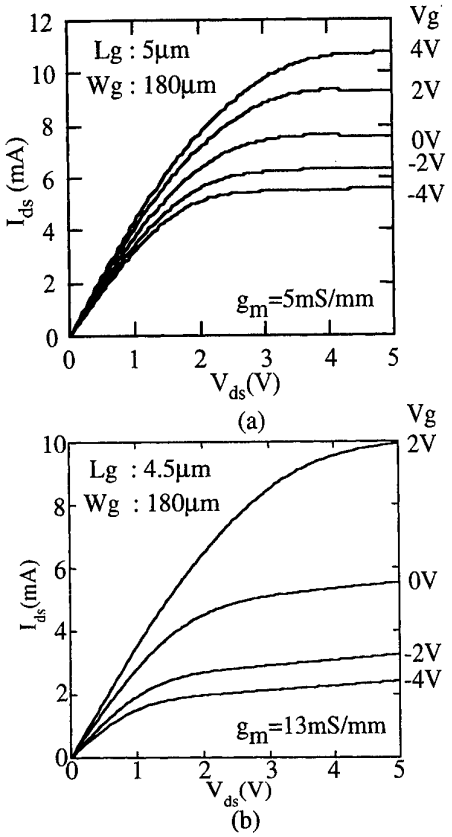

Fig.5. Drain I-V characteristics of the InP MISFETs (a) with *ex-situ* Si ICL process and (b) with *in-situ* Si ICL process.

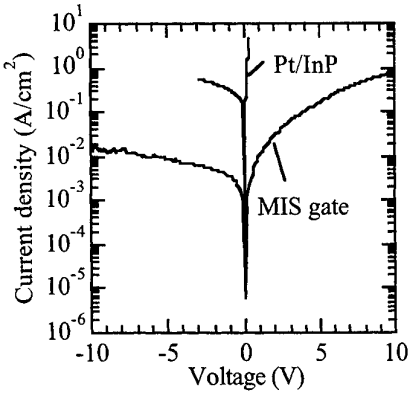

Fig. 6. Gate leakage current characteristics.

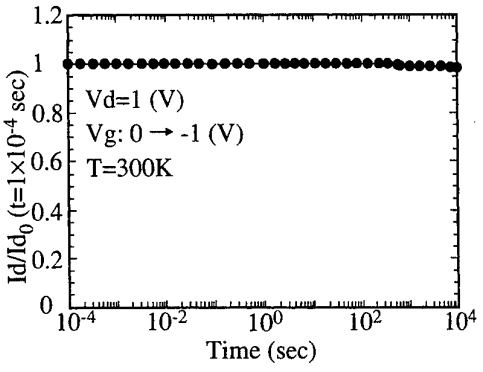

Fig. 7. Drain current drift characteristics of the InP MISFET with *in-situ* Si ICL passivation.

The Recovery Process of RIE damage in InGaAs/AlGaAs PHEMT using Recombination Enhanced Defect Reaction

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The reactive ion etching (RIE) is widely used in GaAs FET process for patterning of dielectric over films such as SiO_2 and Si_3N_4. However, the ion bombardment damage introduced within GaAs active region during the RIE process seriously degrades the device performance. We have found that the RIE damage introduced under the gate region of InGaAs/AlGaAs PHEMT can be drastically recovered by the recombination process for holes at the defect level.

The cross-section of the InGaAs/AlGaAs PHEMT used in this study is shown in Fig. 1. All the layers were grown by MBE. The gate length and width were 1.0 μm and 10.0 μm. After the source and the drain electrodes were deposited on the n^+-GaAs cap layer, the outer recess was formed using H_3PO_4-based etchant. Next, the SiO_2 film of 0.1 μm-thick was deposited by low-pressure chemical vapor deposition (LPCVD) and the resist pattern for the gate electrode was formed using i-line lithography. Then the SiO_2 opening of 1.0 μm-width was formed by SF_6 based RIE at the pressure of 10 mTorr with the RF power (13.56 MHz) of 30 W. During the RIE step, the damage was introduced within the epitaxial layers. Next, the Au/Pt/Ti gate electrode was formed within the SiO_2 opening following the inner recess etching of about 5 nm deep to control the threshold voltage. Finally the Si_3N_4 passivation film was deposited by plasma chemical vapor deposition (PCVD) at 300°C. In order to investigate an influence of the RIE damage on the device characteristics, the reference device of which damage was recovered by a thermal anneal at 420°C was prepared.

The drain current (Ids) at Vds of 3 V and Vgs of 0 V for the devices with and without the RIE damage were 1.214 mA and 3.347 mA, respectively. This result indicates that the carrier concentration of the two dimensional electron gases was decreased due to the RIE damage. However, we have found that the reduction of Ids due to the RIE damage was recovered after the reverse drain to gate current (Igd) stress. Fig. 2 shows the change of the I-V characteristics before and after the Igd stress of -1 mA/mm for 1 hour. It was found that Ids after the stress was recovered up to 3.354 mA, which was almost the same as that for the reference device. To understand the increase of Ids in relation to the Igd stress, the step stress test was performed. Fig. 3 shows the dependence of the shift of Ids on the amount of the stress (the drain to gate bias, Vgd) in the range between 1 V to -19 V (0.2 V step, 2 minutes at each step). The vertical axis in the figure is normalized with respect to the initial Ids of the reference device. As shown in the figure, it was found that the drain current drastically increased for Vgd over -5 V, although that for the reference device did not show any changing. Fig. 3 shows the diode characteristics between drain and gate. The reverse gate current was increased for Vgd over -5 V. This result clearly shows that the increase of Ids, namely the recovery of the RIE damage, strongly depends on the reverse gate current. It should be noticed that Ids did not change by the forward gate current. Based on those results mentioned, this phenomenon can be understood as a recombination enhanced defect reaction (REDR)[1)-2)]. The REDR is known as the damage recovery process for the GaAs p-n junction diode. The minority carrier injection causes non-radiative recombination with the majority carrier captured in the defect level, and the recombination energy are transferred as local vibration energy to the defect, which helps to decrease the activation energy of the damage recovery. In case of the HEMT used in this study, the recombination of holes generated by the avalanche breakdown is assumed to enhance the recovery of the RIE damage. In order to confirm the REDR phenomenon, the temperature dependence of the Ids recovery rate was measured. Fig. 4 shows the dependence of the shift of Ids on the Igd stress time as a function of the temperature. As increased the temperature, it was found that Ids recovered faster. Fig. 5 shows the Arrhenius plot of the Ids recovery rate with and without the Vgd stress. As shown in the figure, the activation energy for the Ids recovery is drastically decreased to 0.119 eV from 0.531 eV under the Vgd stress. It was also found that the activation energy did not depend on Vgd. This result clearly indicates that the phenomenon is not due to the kinetic energy of hot electrons but to the recombination energy. As a conclusion, it has been confirmed that the recovery of RIE damage in InGaAs/AlGaAs PHEMTs can be enhanced under the reverse gate current due to the REDR of holes generated by the avalanche breakdown under the gate.

Reference:

1) D.V.Lang, L.C.Kimerling, and S.Y.leung: J. Appl Phys. 47, 3587
2) M.Uematsu, and K.Wada: Appl. Phys. Lett. 58, 2015

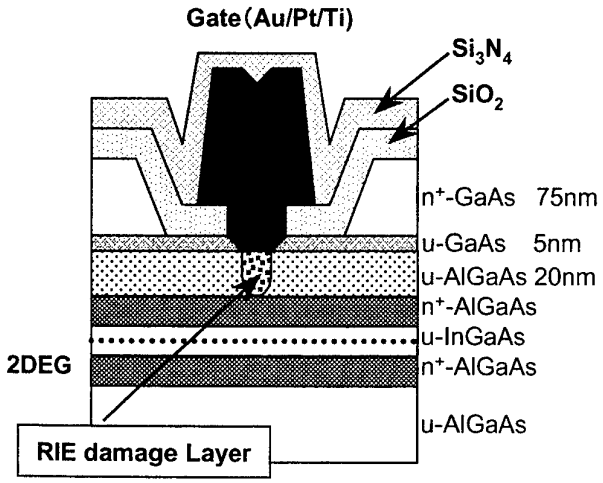

Fig.1
Cross-section of the p-HEMT structure

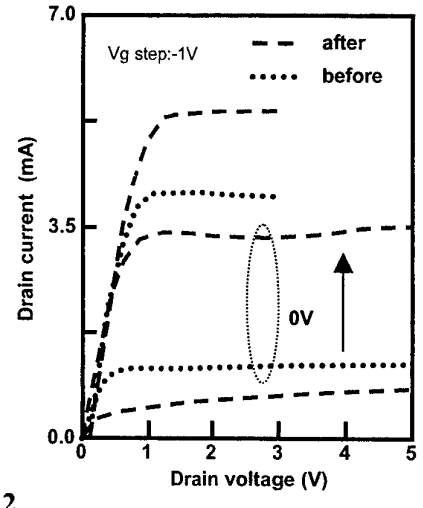

Fig.2
DC characteristics before and after the stress test at Igd of -1mA/mm for 1 hour

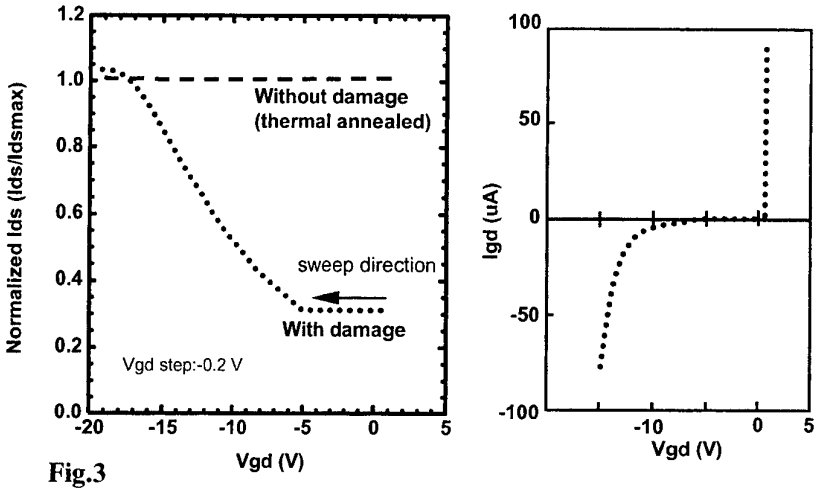

Fig.3
Shift of Ids due to the drain to gate bias for the HEMTs with and without RIE damage (left chart) and I-V characteristics between the gate and the drain (right chart)

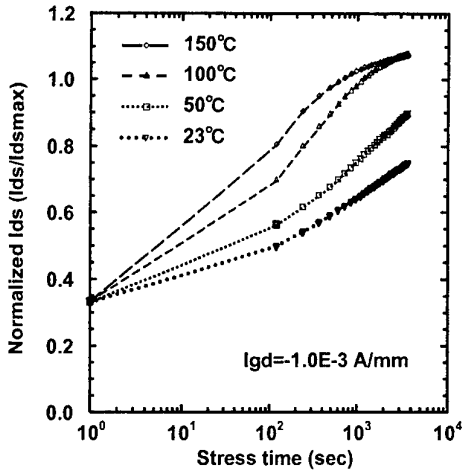

Fig.4
Dependence of Ids recovery rate on the stress time as a function of the test temperature

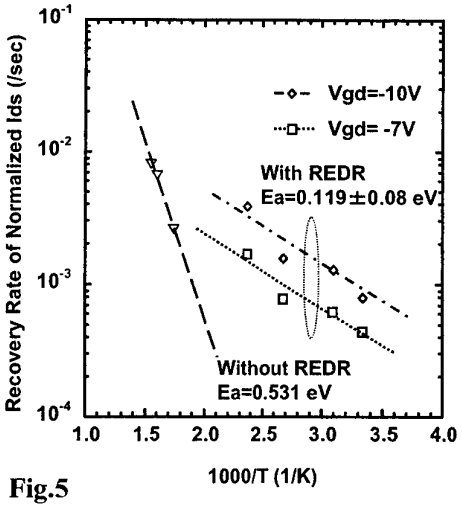

Fig.5
Arrhenius plot of the Ids recovery rate for the thermal annealing and the recombination enhanced defect reaction (REDR)

Suppression of degradation in InP-based HEMTs by inserting InAlP in carrier supply layer

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Abstract

InP-based InAlAs/InGaAs high-electron mobility transistors (HEMTs) are devices of interest for applications in ultra-high-speed digital optical transmission systems due to their high performance. However, some unstable characteristics that severely degrade HEMTs are known. For example, a decrease in drain current or an increase in drain resistance due to accelerated bias-temperature stresses have been reported[1,2]. In this work we present a new structure that improves the degradation of drain resistance and source resistance and lengthens the device life time by about two orders.

A schematic cross section of standard InP-based InAlAs/InGaAs HEMTs is shown in Fig. 1(a). Above the InAlAs carrier supply layer, an InP stopper layer was grown for surface stability on the surface of gate side and for uniformity in the threshold voltage[3]. New HEMTs were formed by simply modifying the standard HEMTs: a thin InAlP layer was inserted in the InAlAs layer on both sides of the δ-doping plane, which is shown in Fig. 1(b).

A typical characteristics degradation example of an InAlAs/InGaAs HEMT, whose initial values for gm, V_{th}, and f_T were 1.0 S/mm, -0.5 V, and 180 GHz, respectively, is shown in Fig. 2(a). After 1000 h of bias-temperature stress of drain-source voltage (Vds) of 1.0 V and gate-sourace voltage (Vgs) of 0.0 V at 195°C, the drain current decreased by half and the device resistance increased. After the same bias-temperature stress of 1000 h was imposed on a new HEMTs, degradation of the drain current was suppressed to about 10% of the initial current and the resistance increase was small, which is shown in Fig. 2(b).

Time dependent changes in source-gate resistance (Rgs) and drain-gate resistance (Rgd) are shown in Fig. 3. The stress conditions were the same as the previous ones. For standard HEMTs, a significant increase in Rgd within 10 h of stresses was observed. Also, an increase in Rgs was observed after 20 h. For new HEMTs, Rgd increased 50~80% after 1000 h of bias-temperature stress. The criteria of life time is defined as the time when Rgd increases by 100% and when Rgs by 10%. The temperature-dependent life time is shown in Fig. 4. For standard HEMTs, the activation energy of the degradation of Rgs and Rgd were 1.9 eV and 1.35 eV, respectively. It is clear that the most critical degradation is an increase in Rgd. The median life time of standard HEMTs will be about $1x10^5$ h at 100°C. For new HEMTs Rgd increase has the same activation energy and the median life time at 100°C is predicted to be about $1x10^7$ h, which is improved by two orders.

In summary, we described a new structure for InP-based HEMTs with InAlP inserted in the carrier supply layer. The life time of the new HEMTs was predicted to be about $1x10^7$ h, which implies high reliability .

References

1) N. Hayafuji et. al., "Degradation mechanism of the AlInAs/GaInAs high electron mobility transistor due to fluorine incorporation," Appl. Phys. Lett. 69 (1996) pp. 4075-4077.

2) A. S. Wakita et.al.,"Drain resistance degradation under high fields in AlInAs/GaInAs MODFETs," IEEE Proc. IPRM, 1997, pp. 376-379.

3) G. Meneghesso et. al., "Elimination of kink effects in InAlAs/InGaAs InP-based HEMT's by means of InP etch stop layer," Inst. Phys. Conf. Ser. No. 162, (1998) pp. 219-224.

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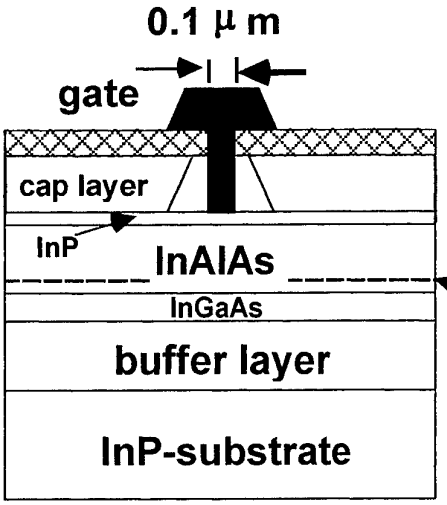

Fig. 1(a) Schematic cross section of standard HEMT.

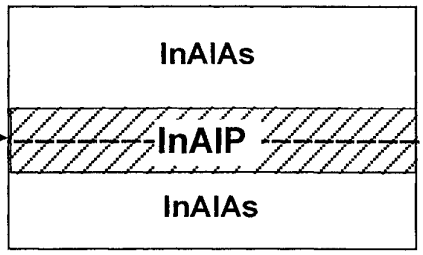

Fig. 1(b) Schematic cross section of carrier supply layer of new HEMT.

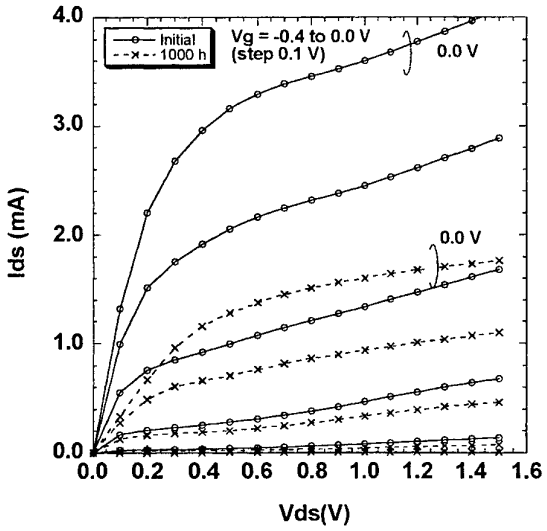

Fig. 2(a) Typical degradation of standard HEMTs due to bias-temperature stress.

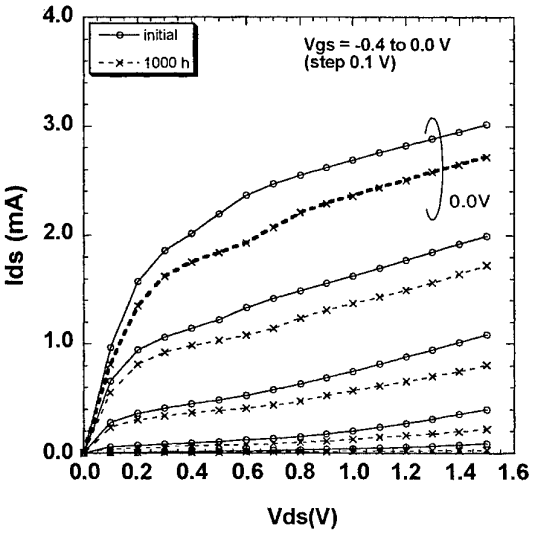

Fig. 2(b) Typical degradation of new HEMTs due to bias-temperature stress.

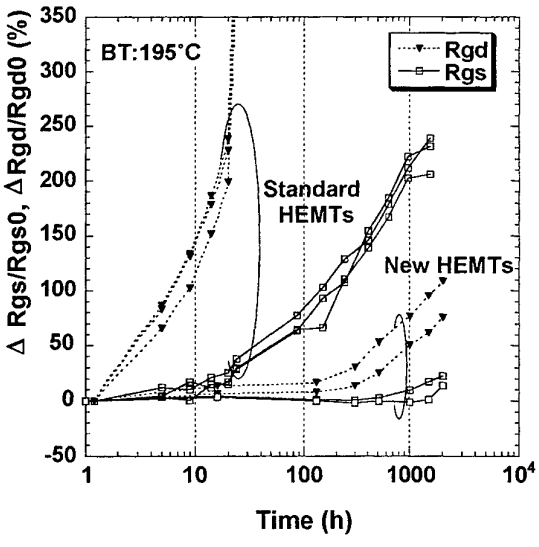

Fig. 3 Time dependent change of Rgs and Rgd for standard and new HEMTs.

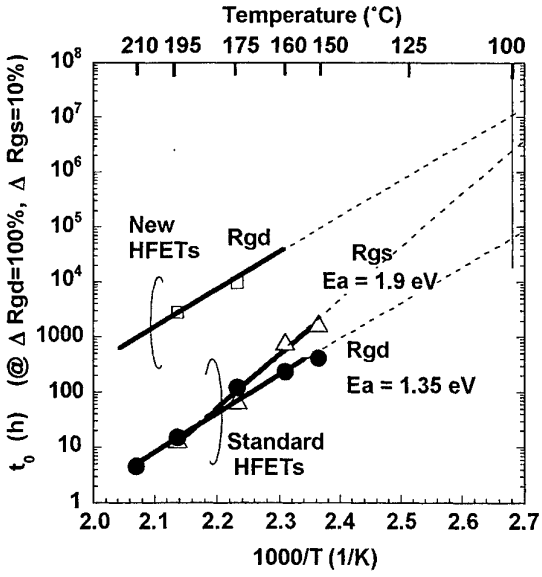

Fig.4 Temperature dependence of median life time for the degradation modes with increases in Rgs (+10%) and Rgd (+100%).

A Light controlled Oscillator using $In_{0.52}Al_{0.48}As$ / $In_{0.80}Ga_{0.20}As$ HEMT

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Introductions: The optical control of microwave and millimeter-wave devices and circuits is an interesting issue due to their potentiality in future's communication systems which connect a high speed wireless communication system and an optical fiber communication system[1],[2]. In order to achieve these systems, a simple opt-electrical transducer must be developed. In this paper, we fabricate the oscillator using $In_{0.52}Al_{0.48}As$ / $In_{0.80}Ga_{0.20}As$ HEMT on InP substrate, and observe the response of the light those amplitude is modulated at high speed .

Device and Circuit Design: The HEMT using in the fabricated oscillator is grown by molecular beam epitaxy (MBE) on InP substrate. The optically-active layer of $In_{0.53}Ga_{0.47}As$ which absorb the 1.55μm light is introduced additionally. The cross-section of the HEMT is shown in Fig.1. This consist of a $In_{0.52}Al_{0.48}As$ buffer layer(100nm), a i-$In_{0.53}Ga_{0.47}As$ absorption layer(80nm), a i-$In_{0.80}Ga_{0.20}As$ channel layer(20nm), a Si-planer-doped $In_{0.52}Al_{0.48}As$ layer (25nm, $N_D=5\times10^{12}/\square$), and a n-doped $In_{0.53}Ga_{0.47}As$ cap layer (25nm). The gate length and gate width are 0.50μm and 50μm, respectively. The surface of the HEMT is covered with Si_3N_4 anti-refraction coat for 1.55μm wavelength. We achieved the negative resistance over 40GHz using this HEMT. The oscillation frequency is designed to be 38GHz.

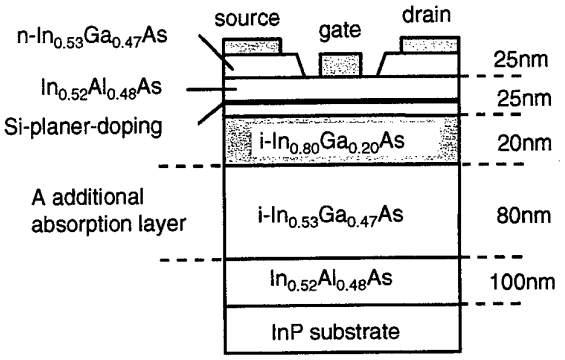

Fig.1 *Cross section of the InAlAs/InGaAs HEMT using in the fabricated oscillator*

Experimental set up: In order to examine the high speed optical response of the oscillator, we constructed the experimental set up of sine-Frequency Modulation(sine-FM).The set up is shown in Fig.2. The amplitude of DFB-laser diode(DFB-LD) output is modulated by the sine-wave from the signal generator. The typical wavelength of DFB-LD is 1.55μm. The modulated frequency and power are 100MHz and +10dBm, respectively. The light is transmitted in the optical fiber(10m), and illuminated on to the surface of the oscillator. The output signal from the oscillator is observed at the spectrum analyzer.

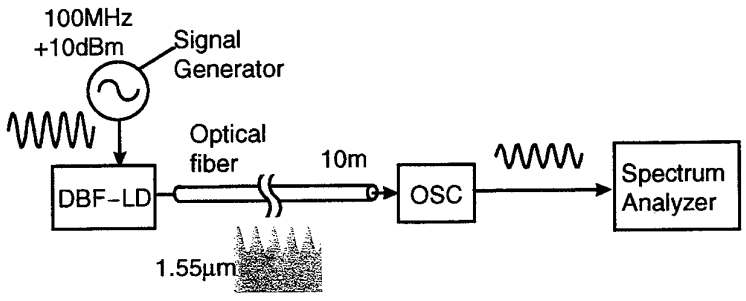

Fig.2 *Experimental set up for optical sine-FM*

Circuit performances: The oscillation frequency and output power of the fabricated oscillator without illumination are 38.9GHz and +8.9dBm, respectively. The frequency shifts as a function of the illuminated optical power(continuos wave)are shown in Fig.3. The downward shifts of the frequency are almost proportional to the incident optical power over 1mW. The amount of shifts does not change as gate bias, and the average slope is -150MHz/mW.

Fig.4 shows the photograph of spectra when the modulated light is illuminated on to the oscillator. The sideband peaks for sine-FM are clearly observed in the regime of 38.6GHz± 100,200,300MHz. Judging from the relative power between center frequency and first sideband peaks, the amount of the frequency shift is estimated to be ~120MHz, i.e, the modulation index is beyond 1 at 100MHz.

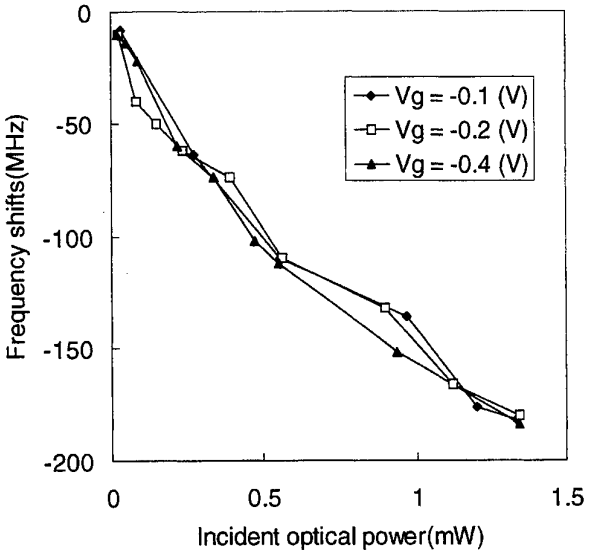

Fig.3 *Frequency shifts as a function of incident optical power*

Discussions: MMIC which transduces optical signal into millimeter-wave has the promising candidates in the field of the communication systems connected a high speed and large volume wireless communication system and a optical fiber communication system. Because of the linearity, the high speed response, and especially the strong output power compared to photodiodes, the fabricated oscillator has a great potential for applying these systems.

Conclusions: We fabricated the light controlled oscillator(1.55μm) those frequency shifts are proportional to the incident optical power over 1mW. Then, optical sine-FM at 100MHz was demonstrated, and the frequency shifts of the fabricated oscillator was estimated to be 120MHz.

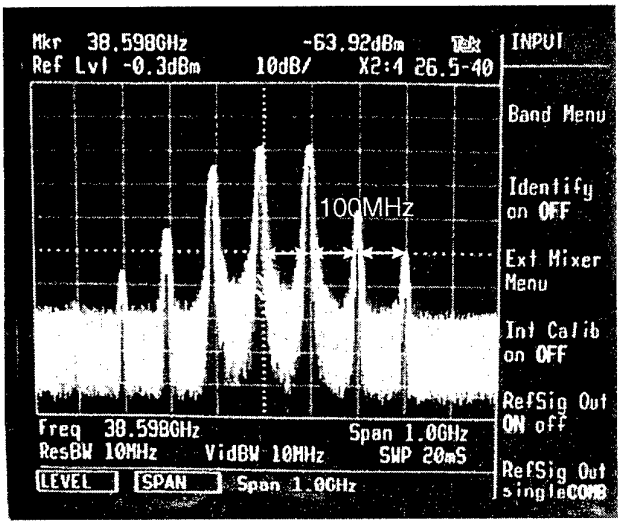

Fig.4 *The measured spectra of the fabricated oscillator under illumination. The amplitude of the light is modulated at 100MHz.*

Acknowledgment: The authors thank S.Kawasaki, a Professor of Tokai University and T.Koya, DENSO CORPORATION for their useful discussions.

References

[1] David Yang, Pallab Bhattacharya, Richard Lai, Timothy Brock, and Arthur Polella, "Optical Control and Injection Locking of Monolithically Integrated $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ MODFET Oscillators," IEEE Trans. Electron Devices., vol.42, pp.31-37, Jan 1995.

[2] Paul Freeman, Xiangkun Zhang, Igor Vurgaftman, Jasprit Singh, and Pallab Bhattacharya, "Optical Control of 14 GHz MMIC Oscillators Based on InAlAs/InGaAs HBT's with Monolithically Integrated Optical Waveguides," IEEE Trans. Electron Devices., vol.43, pp.373-378, March 1996.

AlGaN HEMTs and HBTs for microwave power

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The development of AlGaN/GaN HEMTs has been extremely rapid over the past few years in spite of the limitations of the substrate. The two common substrates of Sapphire and SiC have both large lattice mismatches with GaN and hence result in a large density of threading dislocations. Furthermore the lattice mismatch between AlGaN and GaN also limits the thickness and Al mole fraction in AlGaN/GaN hetrostructures. The need to maximize the Al mole fraction in HEMT structures comes from the need to maximize the two-dimensional electron density arising from the polarization of the lattice. Cree Lighting (fromerly Nitres) has demonstrated 9.8 W/mm power density from optimized AlGaN/GaN HEMTs at X-band. Over 14 W was obtained from a 4mm wide device at 10 GHz. These devices were grown on SiC and thermal management achieved by flip-chip mounting the devices onto inexpensive, thermally conductive, electrically resistive AlN. Widebandwidth circuits using both traveling wave and lossy input match topologies have been demonstrated. Over 5W from 1 to 8 GHz has been achieved using devices fabricated on sapphire substrates.

AlGaN/GaN HBTs and GaN BJTs have been demonstrated using both selectively grown emitters and etched mesa techniques to access the base. A maximum beta of 8 has been achieved in Common Emitter operation at room temperature. The negative impact of dislocations on the performance of BJTs has been established. The need to improve the lifetime in the base has also been unequivocally determined. Through device optimization a breakdown voltage of over 400V has been achieved.

A comparison of HEMTs and HBTs will be presented

RF characterisation and transient behaviour of AlGaN/GaN power HFETs

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GaN/AlGaN HFETs have attached considerable interest in the last few years for power applications at high frequencies. The considerable effort stems from the unique material properties of the III-Nitride semiconductors in particular the large bandgap, the possibility to grow alternatively GaN and AlGaN layers and the good electron transport properties. The GaN/AlGaN HFET technology offers especially large potential to surpass existing device limitations in RF output power, operation voltage and operation temperature at frequencies up to X-band and above. Indeed impressive high frequency results have been reported recently for GaN/AlGaN HFETs with record power densities up to 9.2 Watt/mm measured at X-Band [1,2]. Though exellent results on III-Nitride based RF devices have been obtained, there are still a couple of essential questions to be answered and solved in the future e.g.:

- Are AlGaN/GaN HFETs a lower cost alternative ($ per Watt) to existing RF power technologies such as GaAs HEMT and HBT? For a variety of applications RF power chip cost play a major role (e.g. active phased array antennas).
- Is it possible to further improve the RF gain of AlGaN/GaN HFETs to compete with existing technologies in the strongly expanding broadband communication market?
- Improvement of the maturity of the GaN/AlGaN technology is one of the key tasks in the near future. The understanding and removal of trap related effects is of utmost importance to eleminate current slump effects in GaN/AlGaN HFETs which have been seen in the past by several groups [3-4].

In this paper we summarize the actual status of the GaN/AlGaN HFET power technology at DaimlerChrysler using high quality structures grown by MOCVD on n+ or semi-insulating SiC supplied by Epitronics. A typical HFET structure consists of a 1-2 μm thick GaN buffer layer and a $Al_xGa_{1-x}N$ barrier donor layer with an undoped spacer (3-5nm) and a Si-doped supply layer. Usually a Al content of 25% was used. For sheet concentrations of 1x1013/cm^2 we obtain mobilities of 1300cm^2/Vs. Small area devices with 0.3μm gate length yield f_T=40GHz and f_{max}=80GHz (s.i. SiC substrate). Load-pull characterisation have been performed on multifinger HFETs up to 20 GHz with e.g. output power levels above 3 Watt cw at 15 GHz for a single 1.6mm device (Fig.1). Though the achieved results are very promising for future applications even above X-Band, the performance of these devices is still hampered by different transient effects. For example, recovery of the drain current after gate voltage pulsing have been studied, revealing different time constants ranging from ms to hundreds of seconds with strong dependency on enviromental conditions (illumination, temperature), magnitude and duration of gate voltage change (Fig.2-3).

References

1. Nitrides R&D Technologies in Compound Semiconductors 6 (1) January/February 2000, p.13
2. S. T. Sheppard, K. Doverspike, W. L. Pribble, S. T. Allen, J. W. Palmour, L. T. Kehias, and T. J. Jenkins, „High-power microwave GaN/AlGaN HEMT's on semi-insulating silicon carbide substrates“, *IEEE Electron Device Lett.*, vol. 20, pp. 161-163, 1999.
3. S. Trassaert, B. Boudart, C. Gaquiere, D. Theron, Y. Crosnier, F. Huet, M.A. Poisson " Trap effects studies in GaN MESFETs by pulsed measurements", *Electron. Lett.*, vol. 35, no. 16, 1386-1388, 1999.
4. R. Dietrich, A. Vescan, A. Wieszt, H. Leier, K.S. Boutros, J.M. Redwing, K. Kornitzer, R. Freitag, T. Ebner, K. Thonke" Effect of illumination on the electrical characteristics of AlGaN/GaN FETs", Physica Status Solidi (a) 176, p.209-221, 1999

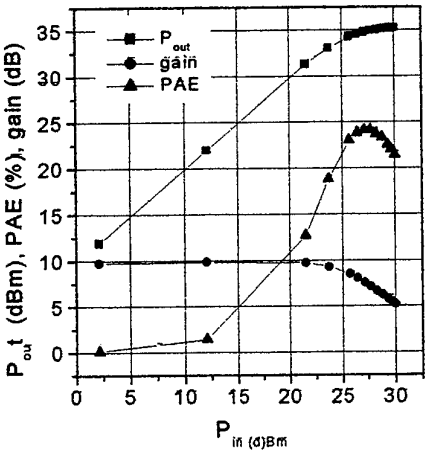

Fig.1: Power measurement result at 15 GHz for a 1.6mm (8x200µm) device biased at Vds=20Volt and Ids=495mA

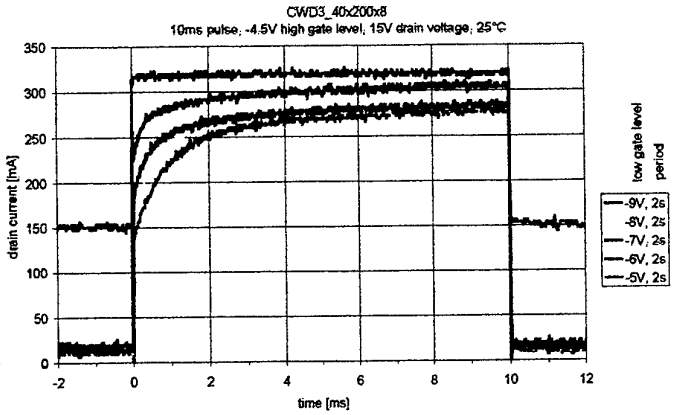

Fig.2: Drain current transients of an AlGaN/GaN HFET after switching of the gate bias from -5,-6,-7,-8,-9Volts to -4.5Volt (Vds=15Volt)

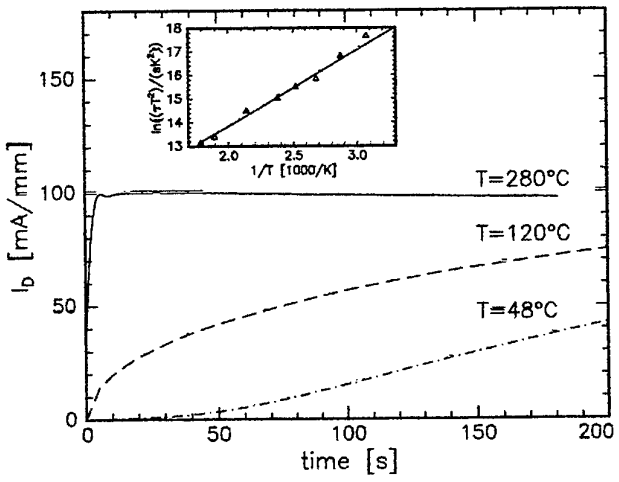

Fig.3: Drain current transients measured at different temperatures for Vgs=1Volt and Vds=6Volt after applying Vgs=-10Volt for 5min. The insert shows the Arrhenius-plot of the time constant T.

Power Performance of AlGaN/GaN HJFETs on SiC and Sapphire Substrates

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Superior power performance has been demonstrated with AlGaN/GaN heterojunction FETs on SiC substrates[1,2]. Also, DC and pulse I-V measurements have shown that SiC substrates are better than sapphire substrates in terms of the self-heating effect[3]. We fabricated AlGaN/GaN HJFETs on SiC and sapphire substrates and have compared their high-frequency and power performances.

The gate-to-drain two-terminal breakdown voltage (BVgd) — that is, the off-state breakdown voltage — was smaller on SiC substrates than on a sapphire substrate. On the other hand, the on-state breakdown voltage for 1-μm-Ldg FETs was about 30 V on a sapphire substrate and 50 to 60 V on SiC substrates. The better on-state breakdown voltage, in contrast to the off-state breakdown voltage, may have been due to the difference in thermal properties. We measured the S-parameters on 100-μm-wide and 1.2 mm wide FETs. Since an n-type conductive SiC substrate was used, a 100-μm-wide FET on SiC showed a smaller f_T than a corresponding FET on sapphire due to the large parasitic capacitance of the bonding pad. However, the power gain and f_T were the same as on sapphire for a 1.2-mm-wide FET, indicating that the small-signal high-frequency performance of FETs on the two substrates is comparable.

The RF power of packaged chips was measured using a load-pull system at 1.95 GHz. The total gate width was 1.2 mm. Up to Vd of 18 V, FETs on the two substrates had similar power, gain and power-added-efficiency (PAE). Above 18 V, however, the power from the sapphire-substrate-FET saturated and the device broke down at 20 V. The FET on SiC had a nearly linear power increase as the supply voltage increased to 30 V. We obtained power of 3.24 W (2.7 W/mm) and PAE of 47% at Vd of 30 V. The difference in behavior above 18 V may have been due to the thermal properties of the substrates. Using a 4-mm-wide FET on SiC, we obtained an absolute power of 6.1 W (1.5 W/mm) at Vd of 22 V, but the device broke down at this voltage. The thermal susceptibility of wider FETs may be greater.

In conclusion, we confirmed that the difference in the thermal conductivity of the SiC and sapphire substrates causes the higher maximum available power of an AlGaN/GaN FET on SiC.

Acknowledgements

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References

[1] S. T. Sheppard, et al., IEEE Electron Device Lett. , Vol. 20, p.161 (1999)
[2] Y. -F. Wu, et al., 1999 IEDM Technical Digest, p.925 (1999)
[3] R. Gaska, A. Osinsky, J. W. Yand, and M. S. Shur, IEEE Electron Device Lett. , EDL-19, p.89(1998)

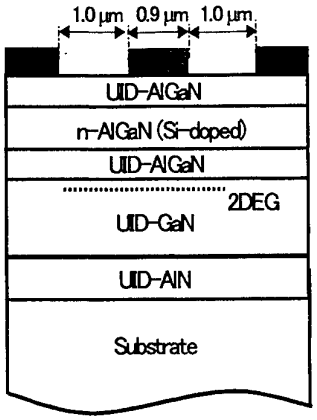

Fig. 1 Schematic cross section of the AlGaN/GaN HJFET

Table. 1 Epitaxial layer structures for FETs on SiC and sapphire substrates.

	on SiC			on sapphire		
LAYER	x for Al	Thick-ness	Conc. (cm^{-3})	x for Al	Thick -ness	Conc. (cm^{-3})
i-AlGaN	0.2	5		0.3	5	-
n-AlGaN	0.2	35	$2x10^{18}$	0.3	15	$4x10^{18}$
i-AlGaN	0.2	5		0.3	5	-
i-GaN	0	3000		0	3000	-
i-AlN	1	100		1	40	-
SUBSTRATE	SiC(4H,6H) (0001) n-type >$5x10^{17}cm^{-3}$			Sapphire (0001)		
V_T (V)	-8			-6.5		
I_{max} (mA/mm)	930			800		
gm_{max} (mS/mm)	120			135		

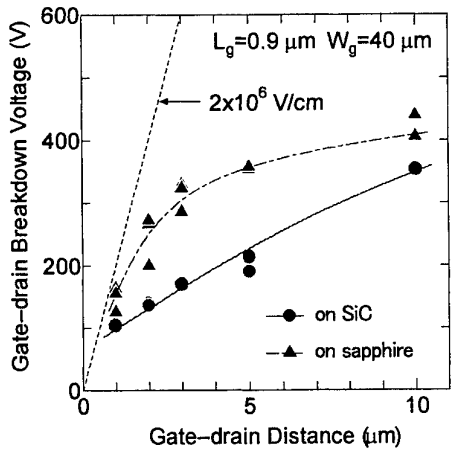

Fig. 2 Gate-drain 2-terminal breakdown voltage as functions of Lgd.

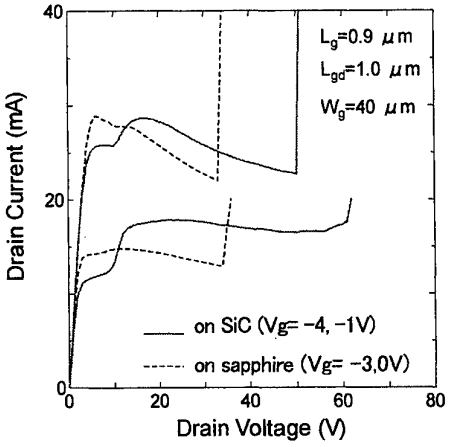

Fig. 3 On-state breakdown characteristics.

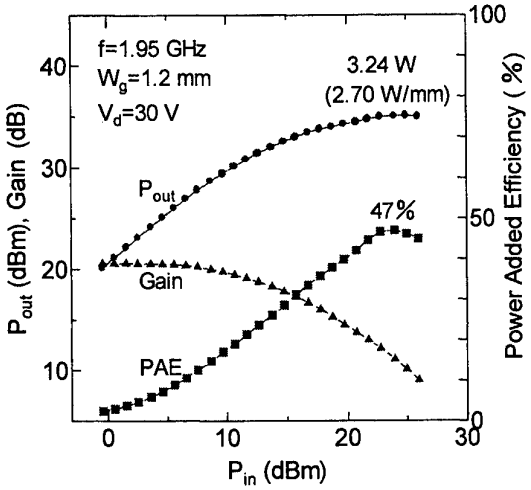

Fig. 4 Output power performance of an AlGaN/GaN FET on SiC substrate. (f=1.95 GHz, Vd=30 V, Wg=1.2 mm)

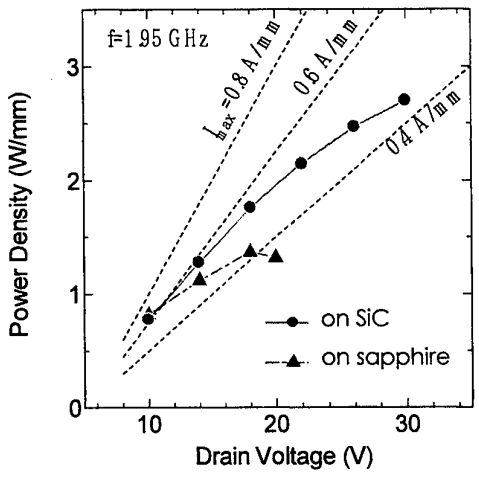

Fig. 5 Output power density as functions of the supply voltage.

AlGaN/GaN epitaxial growth and its application to MODFETs

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AlGaN/GaN MODFETs are useful for devices operating under high-power and high-temperature conditions due to large sheet density, small gate leakage and large breakdown voltage. In fabrication of high-performance AlGaN/GaN MODFETs, it is substantial to reduce parasitic source resistances. To minimize the parasitic source resistances, the recessed gate process has been applied for the GaN-based FET's. Recently, we have shown the transconductance of 146 mS/mm for the AlGaN/GaN MODFET with L_g = 2.1 μm [1]. Further advances in performance of AlGaN/GaN MODFET's are expected to occur with improvements in 2DEG mobility at the AlGaN/GaN heterointerface with low source resistance. In this study we show the transconductance as high as 181 mS/mm and high-temperature characteristics for the recessed gate AlGaN/GaN MODFET on sapphire substrate.

Figure 1 shows the cross-sectional structure of the $Al_{0.26}Ga_{0.74}N$/GaN MODFET grown on a (0001) sapphire substrate by MOCVD. The epitaxial layers consist of a 30-nm-thick GaN nucleation layer, a 2.4-μm-thick undoped GaN layer, a 10-nm-thick AlGaN spacer layer, a 20-nm-thick n^+-AlGaN layer with Si doped to $1x10^{18}$ cm^{-3} and a 20-nm-thick n^+-GaN layer with Si doped to $1x10^{19}$ cm^{-3}. The mesa isolation and the gate recess etch were formed using reactive ion etching in a BCl_3 plasma. The drain-source ohmic contacts were obtained with Ti/Al annealed at 900 °C for 60 sec. The gate metalization was done by vacuum evaporation of Pt/Ti/Au. The gate width was 15 μm and the channel opening (source to drain distance) was 10 μm.

Figure 2 shows the electron mobility and sheet carrier density in the AlGaN/GaN heterostructure as a function of temperature. The electron mobility and the sheet carrier density were 740 cm^2/V-s and $5.1x10^{12}$ cm^{-2} at 300 K, and 12000 cm^2/V-s and $2.8x10^{12}$ cm^{-2} at 8.9 K, respectively. The inset of Fig. 2 shows the magnetoresistance (R_{xx}) from Shubnikov-de Haas (SdH) measurement as a function of magnetic field at 4.2 K. Oscillations are present for fields of 3.8 T and the minima of the oscillations decrease as the field increases, which indicates the presence of the 2DEG at the AlGaN/GaN heterointerface. The sheet carrier density calculated from the SdH data was $3.1x10^{12}$ cm^{-2}.

Figure 3 shows the I_{DS}-V_{DS} characteristic for the gate biases V_{GS} ranging from +1.5 to -6.5 V at 25 °C. The maximum transconductance g_{mmax} and I_{DSmax} as high as 181 mS/mm and 1120 mA/mm were obtained for the recessed gate AlGaN/GaN MODFET with L_g = 1.5 μm, respectively. The g_{mmax} and I_{DS} as a function of temperature are shown in Fig. 4 for the MODFET with L_g = 2.1 μm. The g_{mmax} decreased rapidly from 146 mS/mm at 25 °C to 81 mS/mm at 200 °C, and the decreased gradually to 62 mS/mm at 350 °C. The I_{DS} also decreased with increasing the temperature. The decrease in the transconductance at high temperatures is probably due to the reduction of 2DEG mobility. Figure 5 shows the dependence of V_{th} on temperature for the GaN MESFET and AlGaN/GaN MODFET on sapphire. The V_{th} decreased from -13.3 V at 25 °C to -18.2 V at 300 °C for the GaN MESFET on sapphire. On the other hand, the V_{th} of the MODFET were -6.8 and -7.1 V at 25 and 350 °C, respectively. Note that the temperature dependence of the V_{th} is very weak for the MODFET. The C-V measurements were performed to study the dependence of V_{th} on temperature. For the GaN-based MESFET, the carrier profile at 300 °C spreads in the low electron concentration level compared with that at 25 °C. This results in the shift of V_{th} of the GaN-based MESFET. On the other hand, the electrons confine into the AlGaN/GaN heterointerface and the profile remains unchanged even at 300 °C, which results in the temperature independence of the V_{th} for the AlGaN/GaN MODFET. The aging test was performed for the AlGaN/GaN MODFET under the conditions of V_{GS} = +1 V and V_{DS} = 15 V at 350 °C in N_2 atmosphere. The device exhibited the stable operation with g_{mmax} = 62 mS/mm and I_{DS} = 347 mA/mm over 500 h at 350 °C.

In summary, we have improved the characteristics of the MOCVD-grown AlGaN/GaN MODFET's on sapphire using the process of recessed gate. The recess etched AlGaN/GaN MODFET showed the large g_m of 181 mS/mm and the high I_{DS} level of 1120 mA/mm for the gate length of 1.5 μm. The device exhibited the stable operation at 350 °C for 500 h with the temperature independence of the V_{th}.

Reference: [1]T. Egawa, H. Ishikawa, M. Umeno and T. Jimbo, Appl. Phys. Lett., Vol. 76, p. 121 (2000).

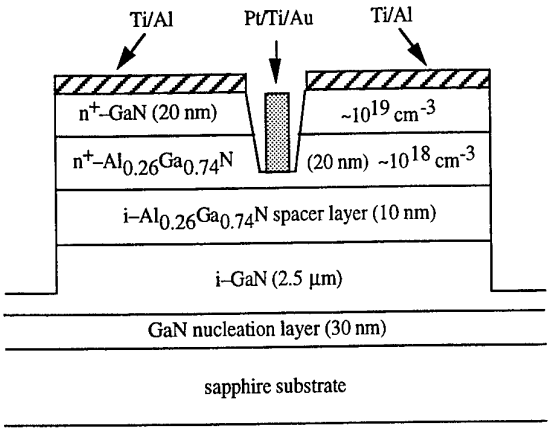

Fig. 1. Cross-sectional structure of recessed gate $Al_{0.26}Ga_{0.74}N$/GaN MODFET grown on sapphire by MOCVD.

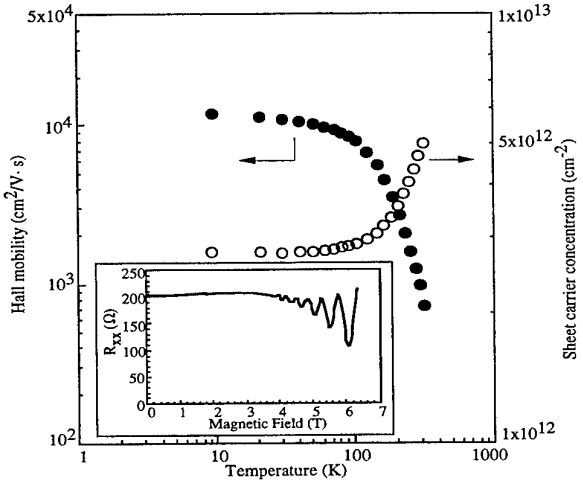

Fig. 2. 2DEG mobility and sheet carrier density as a function of temperature for the AlGaN/GaN heterostructure. Inset shows the magnetoresistance R_{XX} as a function of magnetic field at 4.2 K.

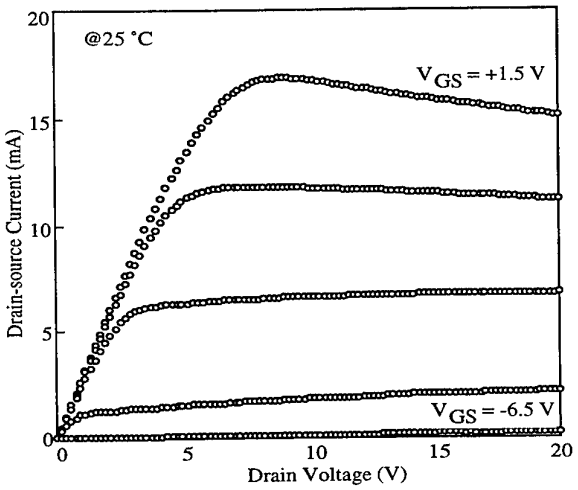

Fig. 3. I_{DS}-V_{DS} characteristic of AlGaN/GaN MODFET at 25 °C. The gate length and width are 1.5 and 15 μm, respectively.

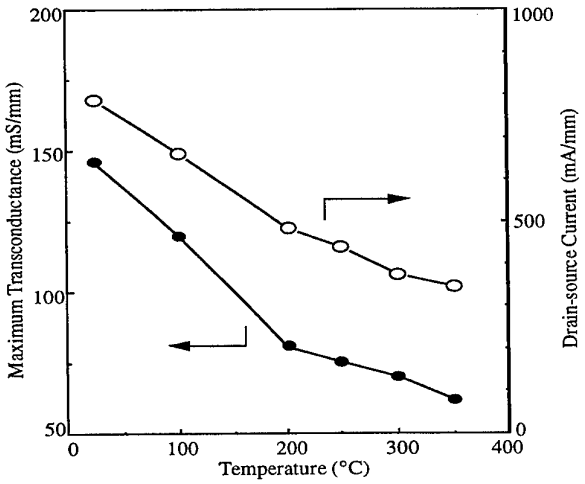

Fig. 4. Transconductance g_m and drain-source current I_{DS} as a function of temperature for the AlGaN/GaN MODFET with L_g = 2.1 μm.

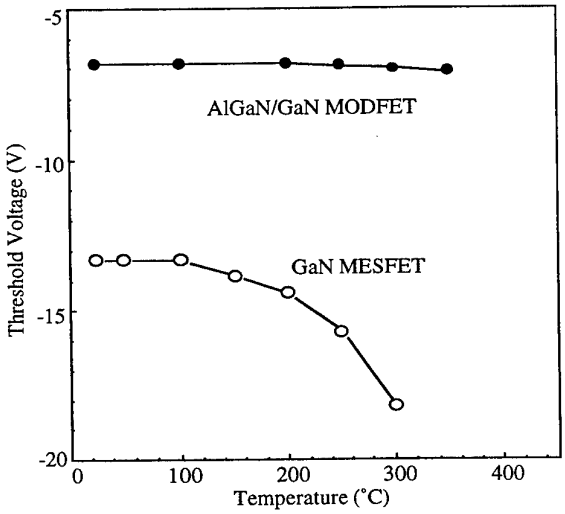

Fig. 5. Dependence of V_{th} on temperature for the GaN MESFET and AlGaN/GaN MODFET on sapphire.

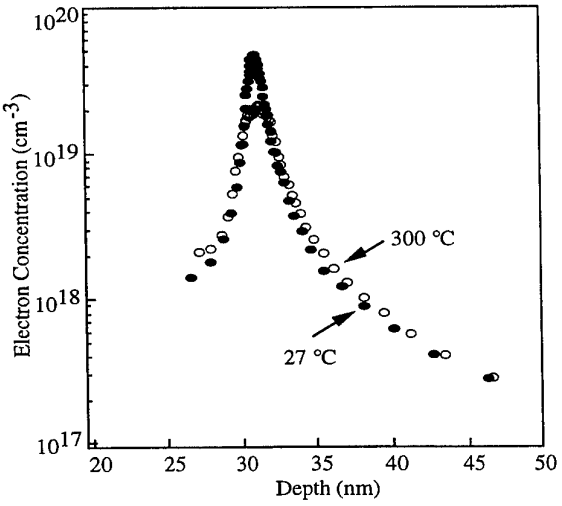

Fig. 6. Carrier concentration profiles measured by C-V method at 25 and 300 °C for the AlGaN/GaN MODFET.

Growth of Si delta doped GaN by metalorganic chemical vapor deposition

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The optical-devices based on III-nitride semiconductors have been rapidly progressed as short-wavelength light-emitting diodes and laser diodes. Due to their high electron saturation velocity and high chemical stability, group III nitrides also have become the most promising material for high temperature and high power field effect transistors (FETs), including metal-semiconductor field effect transistor and high electron mobility transistors (HEMTs). Si δ-doping III-V compound semiconductor such as GaAs and InGaP have been well studied for improving the performance of HEMTs.[1)] Moreover, the incorporation of δ-doping into the laser structure of GaAs-based semiconductors has demonstrated some important improvements in the laser's performance.[2,3)]

In this study, we report a study of parametric dependencies of carrier in Si δ-doped GaN. The parameters include δ-doping time and SiH_4 flow. The C-V profiling technique was employed to investigate carrier density and distribution of the Si δ-doped GaN. We found that the Si δ-doping in GaN and GaAs is not different, except that the carrier distribution is broaden in GaN caused by Si diffusion due to the high growth temperature of GaN.

The samples for this study were grown by a horizontal atmospheric pressure MOCVD on (0001) sapphire substrates. Trimethylgallium (TMG), ammonia were used as precursors with H_2 as a carrier gas, and 10 ppm silane (SiH_4) diluted in H_2 was used as doping precursor. The substrate was first cleaned in flowing H_2 at 1100°C, and then temperature was reduced to 500°C for the growth of a nominal 30-nm-thick GaN layer. Si δ-doping was induced, after a 1.5-μm-thick undoped GaN with 3 μm/h growth rate was grown at 1080°C. The growth process of Si δ-doped GaN is similar to that of GaAs,[4)] the delta doping was achieved by a so-called "interruption-growth procedure", that the detail growth procedure of a δ-doping layer in GaN was as following. Firstly, the growth process of the undoped GaN layer was interrupted by venting TMG flow and following a 10 s H_2 pre-δ-doping purge step, while ammonia continuously flowing through out the process. Then, SiH_4 flow was introduced into the reactor for a certain period of time (δ-doping time) to δ-dope non-growing GaN surface. Finally, SiH_4 flow was stopped and TMG flow was started into

the reactor to resume growth of a 0.2-μm-thick undoped GaN cap layer. Al/Ti guard ring ohmic contact was formed, and Schottky barriers was formed by depositing Pd pads (400 μm diameter) in the guard ring. The ohmic contact metals were alloyed at 650°C for 30 sec. The carrier profiles of Si δ-doped GaN was measured using C-V profiling technique at 300 K and 1 MHz.

C-V profiles of the Si δ-doped GaN with 2 and 5 sccm SiH_4 flow rate and 60 s doping time are shown in Fig. 1. Carrier distribution is usually affected by the dopant diffusion and segregation. Even if the growth temperature is as high as 1080°C, the C-V measurements show high peak carrier density and narrow full width at half-maximum (FWHM), that are completely comparable with the values for Si delta-doped GaAs which have a growth temperature from 550 to 700°C. In addition, the change of carrier density was not observed between with and without post-purge step. It indicates that the thermal decomposition efficiency is small for Si doping in GaN. Also, we do not observe significantly asymmetric broadening of the carrier profile towards the surface direction induced by segregation. The carrier distribution of Si delta doped GaN within a few atomic monolayers was obtained. The saturation of sheet carrier was observed with increasing doping time around $7x10^{12}$ cm^{-2}.

In summary, Si delta-doped GaN was grown by metalorganic chemical vapor deposition, a very high peak carrier density and narrow C-V FWHM of carrier profile was obtained. The C-V FWHM decreases with both increasing the doping time and SiH_4 flow rate. The Si delta doping properties in GaN were similar to that of in GaAs, but FWHM of carrier profile in GaN was broadened that may be due to Si diffusion at considerably high growth temperature in GaN.

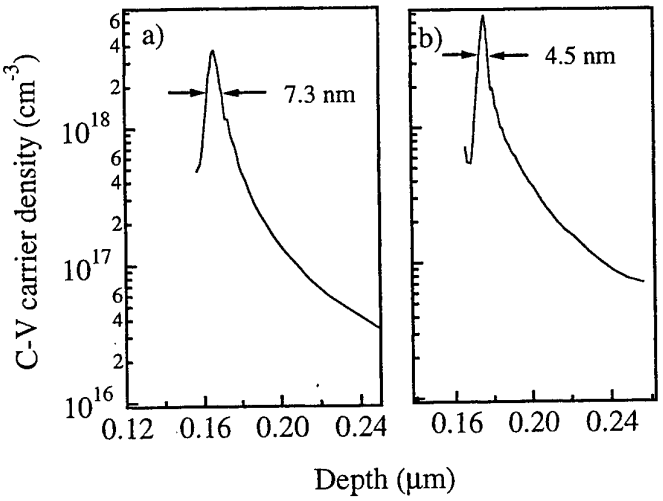

Fig. 1. C-V profile of Si delta-doped GaN grown with the doping time 60 s at different SiH4 flow rate a) 2 sccm, b) 5 sccm.

[1] E. F. Shcubert, J. E. Cunningham, W. T. Tsang and G. L. Timp, Appl. Phys. Lett. **51**, 1170 (1987).

[2] O. Buchinsky, M. Blumin, R. Sarfaty, D. Fekete, I. Samid and M. Yust, Appl. Phys. Lett. **68**, 2043 (1996).

[3] O. Buchinsky, M. Blumin, R. Sarfaty, D. Fekete, I. Samid and M. Yust, Appl. Phys. Lett. **72**, 1484 (1998).

[4] G. Li and C. Jagadish, J. Cryst. Growth, **111**, 239 (1991).

Surface Passivation Process for GaN-Based Electronic Devices Utilizing ECR-PCVD Si_3N_4 Film

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GaN-based field-effect transistors (FETs) including high-electron mobility transistors (HEMTs) utilizing AlGaN/GaN hetreostructures have demonstrated their high potential for high-power microwave electronics. Due to existence of intrinsic and piezoelectric polarization charge, surface-state-free and reproducible surface passivation is practically indispensable for stable operation of such devices. However, little is known about surface and interface properties of GaN-based material system so far.

In this paper, an attempt was made to develop the surface passivation process for GaN-based electronic devices utilizing ECR-PCVD Si_3N_4 film. Interface properties of GaN MIS structures were systematically investigated with a special focus on the effect of various types of surface treatments.

Figure 1 shows a schematic illustration of the fabricated MIS structures. Si-doped GaN epitaxial layers ($n=1\text{-}3\times10^{17}$ cm^{-3}) were grown on sapphire substrates by metal organic vapor phase epitaxy (MOVPE). In view of actual device fabrication process, surface processes included a simple wet treatment in NH_4OH solution at 20 - 50°C for 5-15min followed by the dry processes for 1-5 min using the ECR-N_2 plasma with a power of 50W or the H_2 plasma with a power of 100W. Then, SiO_2/n-GaN and Si_3N_4/n-GaN structures were prepared by rf-plasma CVD using N_2O and SiH_4, and by ECR plasma CVD using N_2 and SiH_4, respectively.

Typical AFM images of the GaN surfaces before and after the surface treatments were shown in **Fig. 2**. The NH_4OH treatment completely maintained the surface smoothness. Comparable RMS values of surface roughness were obtained even after the plasma treatment process. These surface treatments were found to be effective in reduction of natural oxide layer of GaN surfaces, which was confirmed by detailed XPS measurements.

Figure 3 shows Raman spectra taken at room temperature from the GaN surfaces before and after the deposition of a Si_3N_4 film. For the NH_4OH treated GaN surface, the E2 line was clearly detected at 568 cm^{-1} which is very close to that reported by Link et al [1]. No change in the peak position and the line width of the E2 mode was observed after the Si_3N_4 passivation by ECR plasma process, indicating that no pronounced stress took place at the Si_3N_4/GaN interface.

Figure 4 summarizes typical C-V characteristics of the GaN MIS structures. Poor C-V behavior was observed for the SiO_2/GaN sample, reflecting the existence of high density of interface states. In contrast, the ECR-CVD prepared Si_3N_4/GaN structures showed better C-V characteristics, as shown in **Figs. 4 (b) and (c)**. The measured C-V curves were very close to the calculated ones, and clear deep depletion behavior was observed at room temperature, similar to that of wide-gap semiconductor MIS structures such as SiO_2/SiC[2]. **Figure 5** shows distributions of interface state density (D_{it}) of the fabricated MIS structures. The Si_3N_4/GaN structures showed relatively low density of interface states, as compared to the SiO_2/GaN interface. Furthermore, surface treatment processes using the ECR plasma achieved lower D_{it} value of 2×10^{11} cm^{-2} eV^{-1}. This seems to be related to the removal of natural oxides from GaN surfaces, as confirmed by XPS measurement. However, the long-time plasma treatment was found to introduce a discrete defect state peak near Ec on the GaN surface probably due to the plasma damage, as seen in the 5-min data in Fig.5.

Thus, the present ECR deposition of Si_3N_4 films combined with a suitable surface treatment is promising for the successful surface passivation of GaN-based electronic devices.

[1] A. Link et al., J. Appl. Phys., **86**, 6256 (1999).
[2] J. Tan et al., Appl. Phys. Lett., **70**, 2280(1997).

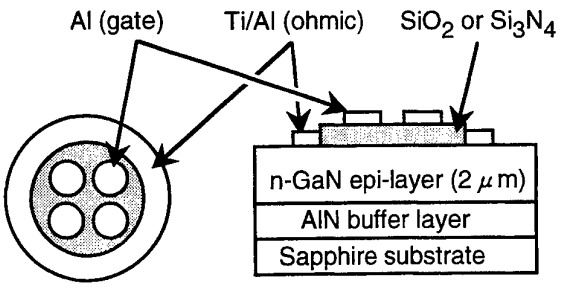

Fig. 1 MIS sample structure.

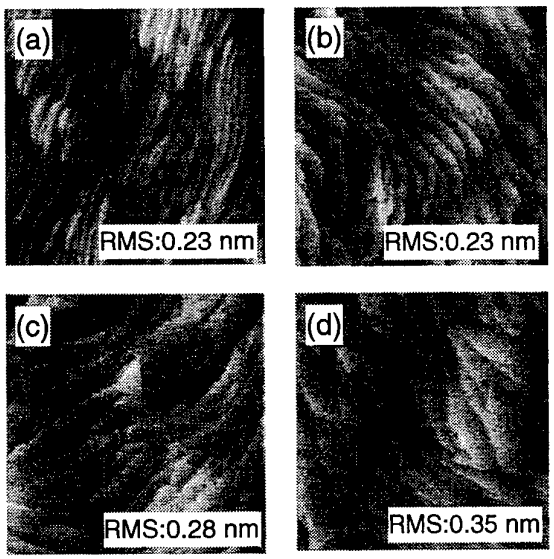

Fig. 2 AFM images of GaN surfaces treated in (a) organic solvents, (b) NH_4OH solution, (c) NH_4OH solution and H_2 plasma, and (d) NH_4OH solution and N_2 plasma.

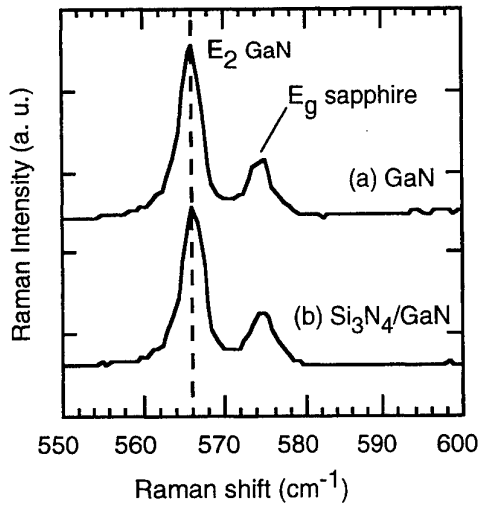

Fig. 3 Raman spectra from (a) NH_4OH-treated GaN surface and (b) Si_3N_4/GaN structure.

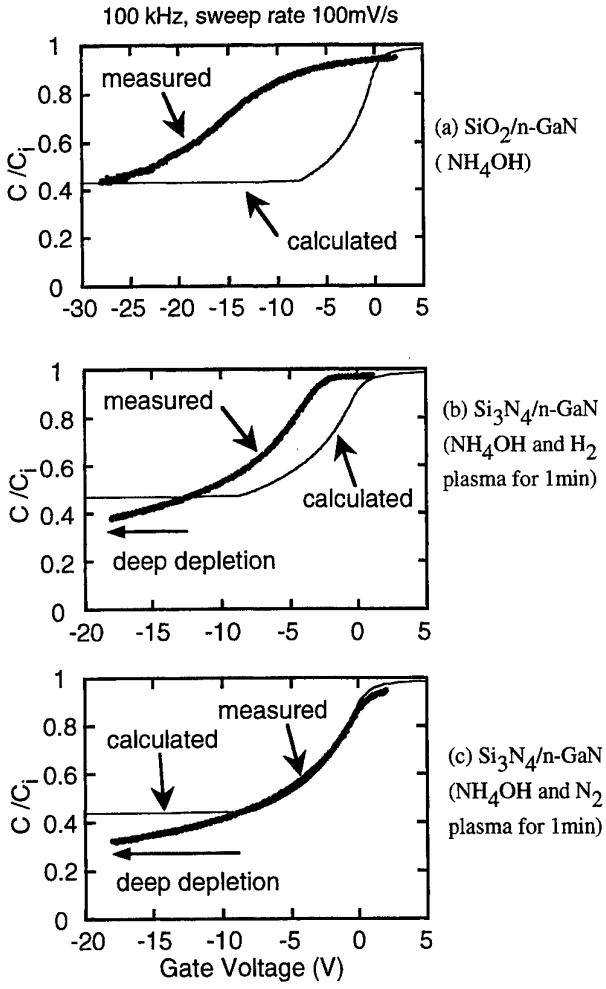

Fig. 4 C-V curves of SiO_2/n-GaN and Si_3N_4/n-GaN structures.

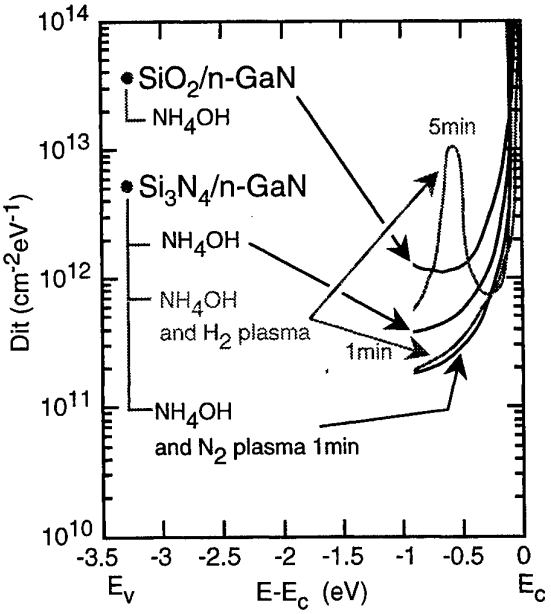

Fig. 5 Distributions of interface state density for the fabricated MIS structures.

GaN-based Gunn Diodes: Their Frequency and Power Performance and Experimental Considerations

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Recent advances in the area of nitride-based wide-bandgap semiconductor technology allowed demonstration of new generation devices with high power capability. Discrete GaN-based HFETs with *10W* of output power at X-band have been recently demonstrated [1]. At the same time, electron transport in III-V nitrides is expected to have some common features with GaAs- and InP-based materials. Thus, studies of fundamental properties in GaN indicate that this material also exhibits Negative Differential Resistance (NDR) and as a result, electrons exposed to high electric field experience negative differential mobility. However, the threshold field for NDR in GaN appears to be as much as *40* times higher than in GaAs (F_{TH}=*150KV/cm* vs. *3.5KV/cm*) [2].

Gunn diodes made of conventional III-V compound semiconductors have been successfully applied for generation of high-power millimeter-wave signals using oscillators based on the NDR effect [3, 4]. The frequency capability of such Gunn-diode oscillators is limited by the energy-relaxation time in the semiconductor material since the NDR effect disappears when the period of oscillations is shorter than the intervalley electron transfer time. Monte-Carlo studies of high-field electron transport in GaAs and GaN [5], estimated the energy-relaxation times (τ) in these materials and a much shorter time (τ_{GaN} *~1.2ps*) was found in GaN than in GaAs (τ_{GaAs}=*7.7ps*) [6]. Based on the above considerations, it appears therefore that use of GaN with increased electrical strength and reduced electron-transfer time constants offers the possibility to increase the operation frequency, as well as, the power-capability of NDR diode oscillators and extend the range covered by more traditional III-V semiconductor-based generators to THz frequencies.

Large-signal power analysis of Gunn diode oscillators was performed by introducing boundary conditions to represent the *LCR* oscillator cavity in which the diode was inserted. The regions of voltage *V(t)* and current *I(t)* waveforms corresponding to sustained oscillations were subjected to harmonic analysis and the resulting power spectrum was used to determine the frequency and power of the Gunn diode oscillators. The approach of this study was verified by simulating the performance of Ka-band GaAs Gunn diode oscillators. The simulations showed that the operation frequency of GaAs Gunn diodes was approximately *40GHz*, while the output power was about *10dBm* in good agreement with the expectations for this design [7]. GaN Gunn diodes with the same thickness and diameter showed significant improvement over GaAs devices in terms of output power density and frequency in agreement with the signal-generator figure-of-merit Pf^2Z [3], which is *100* times higher for GaN.

A THz diode design having a thinner active layer (*0.3μm*) and, thus, expected to operate at a higher frequency was used to further investigate potential of GaN-based Gunn diodes for THz power generation. The power spectrum of the THz GaN Gunn oscillator showed operation frequency of *774GHz* and conversion efficiency of *0.7%* . This high frequency capability of GaN is due to high carrier velocity, short relaxation times and large threshold field in this material.

GaN Gunn diode layers were grown by in-house MOCVD. The active layer doping varied between 1×10^{17} cm^{-3} and 5×10^{17} cm^{-3} while the thickness was 2.5 μm to 3.0 μm. Cl-based

RIE was used for etching while ohmic contacts were made of Ti/Al/Ti/Au. GaN diodes were tested using a pulsed setup and their characteristics were compared with those of GaAs diodes. The GaN-based diodes showed larger voltage and current capability and their operation was limited by heating. Overall, we present the frequency and power characteristics of GaN-based Gunn diodes and discuss their process and first experimental evaluation.

Work supported by ONR (Contract No. N00014-92-J-1552) and DARPA/ONR (Contract No. N00014-99-1-0513)

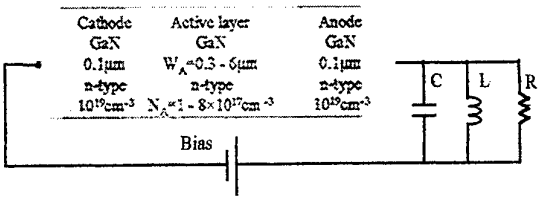

Fig.1. Schematic of GaN NDR diode oscillator showing the cross-sectional design of GaN NDR layers, bias supply, and an equivalent-circuit representation of the resonant cavity

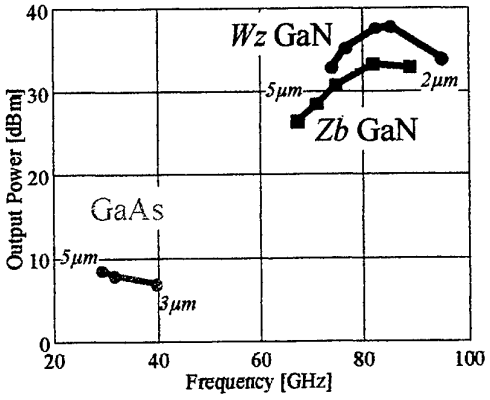

Fig.2. Concentration-frequency diagram illustrating frequency capabilities of NDR diodes made of GaAs and GaN

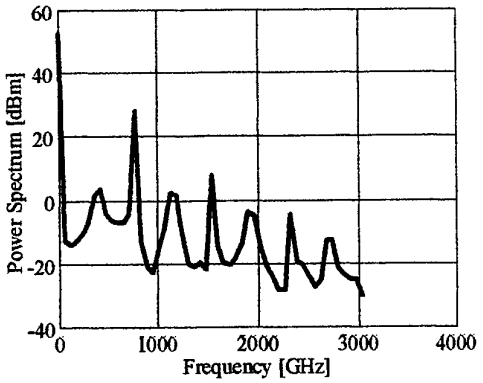

Fig.3. Simulated output power spectrum of *0.3μm*-thick GaN-based NDR diode oscillator designed for operation at THz frequencies.

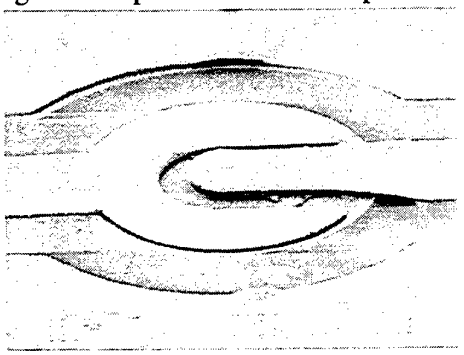

Fig.4. Fabricated GaN NDR Diode with air-bridge interconnects

References

[1]Press release "Nitres Reports 14 W GaN-based HEMT Amplifier", www.compoundsemiconductor.net Oct. 1999

[2] J. Kolnik et al., *J. Appl Phys*, 78 (2), p 1033-1038, July 1995

[3] P. J. Bulman, G. S. Hobson, B. C. Taylor, "Transferred Electron Devices", Academic Press, New York, 1972

[4] H. Eisele and G. I. Haddad, *IEEE Microwave and Guided Wave Letter*, vol.8, no.1; p.24-6, Jan. 1998

[5] B.E.Foutz et al., *Appl Phys Lett.* 70 (21), p 2849-52, 1997

[6] E. Alekseev, D. Pavlidis, *Solid-State Electronics*, Vol. 44, n.6, pp 941-947, 2000

[7] T. G. Ruttan, *IEEE Transactions on Microwave Theory and Techniques*, p 142-144, February 1974

Quasi-optical coherent power combiners for the short-millimeter and submillimeter wave region

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1. Introduction

Short-millimeter and submillimeter waves remain as undeveloped electromagnetic spectra, mainly due to lack of practical coherent sources. Recent advances in heterostructure microelectronics have thrown slightly light to the frequency regions by providing HEMT's and HBT's with the maximum oscillation frequency above 200 GHz [1-2]. However, their output power is still not enough for practical applications, and decreases quickly as the frequency increases. The limited power-handling capability of the solid-state devices, along with downward trend with frequency, is a fundamental limitation [3]. Spatial power combining of large numbers of the devices using a quasi-optical resonator is a promising technique that enables these devices to generate intense continuous waves even at the submillimeter wavelengths [4]. In this paper, we present quasi-optical power combiners using solid-state devices and related circuit techniques.

2. Quasi-optical oscillators

Connecting a number of devices in parallel or series is the most common way to combine the power of devices, such as a multiple gate-finger HEMT. This circuit-based power combining, however, encounters difficulties at the short-millimeter wave frequencies where transmission losses are more conspicuous. Quasi-optical or spatial power combining of devices have been developed to circumvent the problem.

Figure 1 shows one of the very first demonstrations of coherent power combining arrays using a quasi-optical resonator [5-6]. The resonator consists of a concave mirror and a metal grooved mirror on which three terminal devices or two terminal devices are mounted. This Fabry-Perot resonator can achieve a high Q-value at high frequencies even in the submillimeter wave region, and its size enables a number of oscillator elements in the resonator. In addition, the resonator configuration shown in Fig. 1 has large heat dissipation power which enable the mounted devices to withstand for CW-operation with high output power.

Coherent power combining of multi-elements in a resonator not only increases the outpu power, but also improves the carrier to noise (C/N) ratio of an oscilla-

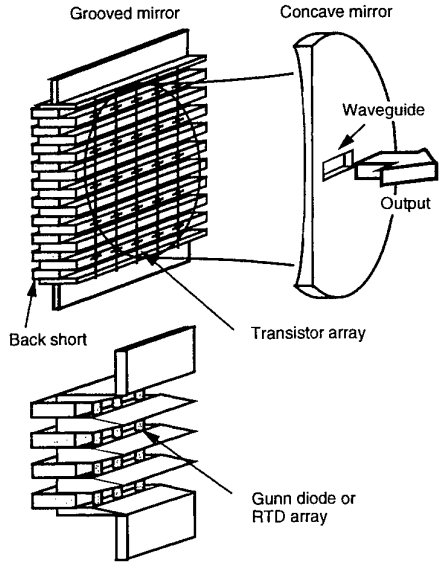

Fig. 1 Quasi-optical resonator with multi-oscillator elements.

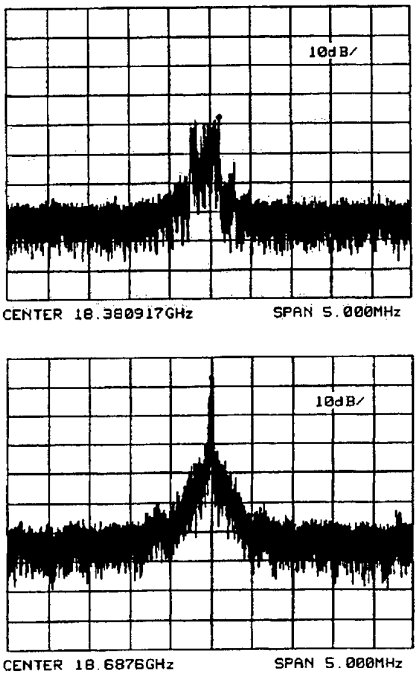

Fig. 2 Measured frequency spectra of the quasi-optical oscillator with (a) one HEMT and with (b) 36 HEMT's.

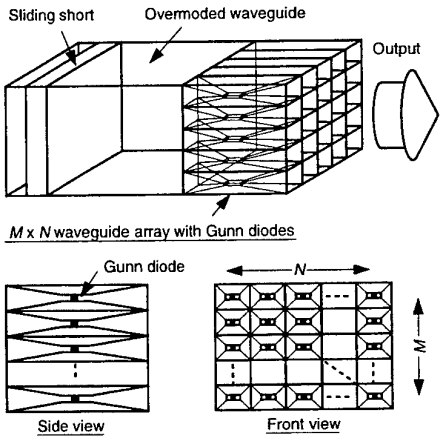

Fig. 3 Overmoded-waveguide oscillator with an *MxN* Gunn diode array.

tion spectrum. Figure 2 compares the measured spectrum for one HEMT with that for 36 HEMT's in the Fabry-Pero resonator at about 18 GHz. The results clearly show that the high C/N ratio can be achieved in the power combining type oscillator.

A resonant tunneling diode (RTD) is a promising device to be able to oscillate at the frequencies above 700 GHz but its power is typically several tens of microwatts. We have demonstrated experimentally our resonator can be used to combine coherently power of GaAs/AlAs -RTD's at 81 GHz [7].

The concept of our oscillator configuration has been extended by another research group to grid oscillator and grid amplifiers where transistors are mounted on a dielectric or semiconductor substrate with antennas and biasing leads [8-9]. A several-watts, 37 GHz monolithic grid amplifier has been demonstrated using a GaAs-pHEMT array with more than 500 elements. Thermal management has been considered on this grid to obtain CW operation. Recently, a 36 W, 60 GHz band quasi-optical amplifier using a multi-layer substrate with 272 HEMT's has also been demonstrated [10].

3. Overmoded waveguide oscillator

Coherent power combiners with overmoded waveguides have been developed to combine power efficiently from several tens of elements at the frequencies below 300 GHz [11]. Figure 3 shows an *MxN* Gunn diode array oscillator in an overmoded waveguide resonator. The oscillator consists of an *MxN* array of fundamental-mode (TE_{10}) waveguides with pyramidal horn couplers at both ends, a metal overmoded waveguide, and a sliding short. The Gunn diodes are mounted at the center of the TE_{10}-mode waveguides. The *MxN* TE_{10}-mode array transfers energy selectively to a TE_{N0}-mode in the overmoded-waveguide through the horn couplers with conversion efficiency of 100 %. So far, the CW output power of 1.5 W at 60 GHz and 0.5 W at 99 GHz have been achieved with this structure containing nine Gunn diodes. Figure 4 shows the measured oscillation

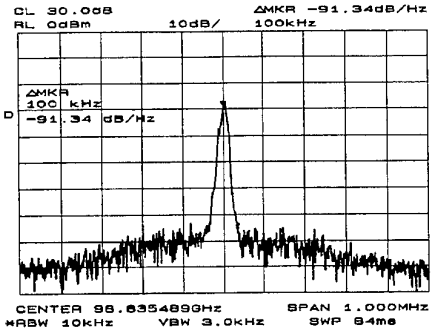

Fig. 4 Measured frequency spectrum of the overmoded-waveguide oscillators with nine diodes.

spectrum with a high C/N ratio of 91 dB/Hz in the oscillator at 99 GHz.

4. Summary

Quasi-optical power combining techniques provide a means to produce coherent and high power solid-state oscillator operating at the short-millimeter and submillimeter frequencies. These oscillators with high performance could develop new applications in this frequency region, exploiting new and rich frequency resources.

REFERENCES

[1] Y. C. Chen, D. L. Ingram, R. Lai, M. Barsky, R. Grunbacher, T. Block, H. C. Yen, and D. C. Streit, "A 95-GHz InP HEMT MMIC Amplifier with 423-mW Power Output," IEEE Microwave Guided Wave Lett., vol. 8, no. 11, pp. 399-401, 1998.

[2] B. Agarwal, Q. Lee, D. Mensa, R. Pullela, J. Guthrie, and M. Rodwell, "80-GHz Distributed Amplifiers with Tansferred-Substrate Heterojunction Bipolar Transistors," IEEE Trans. Microwave Theory Tech., vol. 46, no. 12, pp. 2302-2307, 1998.

[3] R. A. York, in Active and Quasi-Optical Arrays for Solid-State Power Combining, ed. R. A. York and Z. B. Popovic, (John Wiley & Sons, inc., 1997).

[4] J. W. Mink, "Quasi-Optical Power Combining of Solid-State Millimeter-Wave Sources," IEEE Trans. Microwave Theory Tech., vol. MTT-34, no. 2, pp. 273-279, 1986.

[5] K. Mizuno, T. Ajikata, M. Hieda, and M. Nakayama, "Quasi-optical resonator for millimeter and submillimeter wave solid-state sources," Electron. Lett., vol. 24, pp. 792-793, June 1988.

[6] J. Bae, Y. Aburakawa, H. Kondo, T. Tanaka, and K. Mizuno, "Millimeter and Submillimeter Wave Quasi-Optical Oscillator with Gunn Diodes," IEEE Trans. Microwave Theory Tech., vol. 41, no. 10, pp. 1851-1855, 1993.

[7] T. Fujii, H. Mazaki, F. Takei, J. Bae, M. Narihiro, T. Noda, H. Sakai, and K. Mizuno, "Coherent Power Combining of Millimeter Wave Resonant Diodes in a Quasi-Optical Resonator," IEEE MTT-s Int. Microwave Symp, San Francisco, vol. 2, pp.i19-922, 1996.

[8] Z. B. Popovic, M. Kim, and D. B. Rutledge, "Grid oscillators," Int. J. Infrared and Millimeter waves, vol. 9, pp. 647-654, July 1988.

[9] R. M. Weike II, M. Kim, J. B. Hacker, M. P. Delisio, Z. B. Popovic, and D. B. Rutledge, "Transistor Oscillator and Amplifier Grids," Proc. Of the IEEE, vol. 80, no. 11, pp. 1800-1809, 1992.

[10] J. J. Sowers, D. J. Pritchard, A. E. White, W. Kong, and O. S. A. Tang, "A 36 W, V-band, Solid State Source," IEEE MTT-s Int. Microwave Symp, Anaheim, California, MO3C-1, 1996.

[11] J. Bae, T. Unou, T. Fujii, and K. Mizuno, "Spatial Power Combining of Gunn Diodes Using an Overmoded Waveguide Resonator at Millimeter Wavelengths," IEEE Trans. Microwave Theory Tech., vol. 46, no. 12, pp. 2289-2294, Dec. 1998.

High-Speed and High-Output Uni-Traveling-Carrier Photodiode

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The generation of high-speed electrical signals by optical-to-electrical (O/E) signal conversion has the potential of overcoming the speed limit of today's electronics-based technology. To make the signal intensity after the O/E conversion high enough, ultrafast photodetectors with high saturation power levels are essential [1]. The uni-traveling-carrier photodiode (UTC-PD) [2], which has a unique mode of operation, is a promising candidate for such requirements.

Figure 1 shows the band diagram of the UTC-PD. Because the p-type absorption layer is quasi-neutral, majority holes respond very fast, i.e., within a dielectric relaxation time, due to their collective motion. Therefore, only electrons are the active carriers, and their transport determines the total delay time. Since the electron velocity at overshoot is about one order of magnitude larger than the hole saturation velocity, the carrier transit time in the depletion layer is much smaller in UTC-PD than in a conventional pin-PD. The space charge effect in the depletion layer is also much less in the UTC-PD structure.

Figure 2 shows the pulse photoresponse of a back-illuminated InP/InGaAs UTC-PD with an absorption layer thickness (W_A) of 860 A, as measured by the electro-optic sampling (EOS) technique [3]. The Fourier transform of the narrowest pulse response (after a deconvolution) gave a 3-dB bandwidth (f_{3dB}) of 235 GHz [4]. This is the highest f_{3dB} ever reported for a PD operating at a λ of 1.55 μm. The f_{3dB} decreases with increasing input pulse energy or increasing reverse bias voltage, due to the space charge effect and the shift of the electric field value from the optimum velocity-overshoot condition. Nevertheless, an output peak current (I_p) of 30 mA was obtained with an f_{3dB} of 185 GHz. A higher f_{3dB} can be expected by reducing W_A without sacrificing the CR charging time, because the choice of thickness of the depletion layer and that of the absorption layer are independent of each other in the UTC-PD structure [1,5].

Figure 3 shows the photoresponse of a UTC-PD (W_A = 2200 A, 25 Ω load) at the high excitation condition [6]. The I_p exceeds 180 mA when the output pulse-width (FWHM) was kept under 5 ps. This I_p is about an order of magnitude larger than that obtained with conventional pin PDs. The Fourier transform of this pulse response resulted in an f_{3dB} of 79 GHz. Figure 4 plots I_p as a function of input pulse energy (P_{in}) with bias voltage (V_b) as a parameter [7]. Although I_p saturates at higher P_{in} values, it is clear that the region of the linear dependence of I_p on P_{in} expands with increasing V_b and exceeds 80 mA for a V_b of -4 V.

UTC-PDs have a variety of applications. Photo-receiver operation at 80 Gb/s [8], and an optical demultiplexer function at 40 Gb/s in combination with an electro-absorption modulator [9] have already been realized, as have the analog applications of high-power millimeter-wave transmission over +10 dBm at 60 GHz without employing a power amplifier [10] and millimeter-wave imaging at 100 GHz [11]. In particular, the UTC-PD's wide linearity range (Fig. 4) is important for the wireless communication systems. The electrical pulses generated by a UTC-PD have also been used for optoelectronic network analysis based on the EOS technique at frequencies exceeding 300 GHz [12].

References

[1] Y. Miyamoto M. Yoneyama, K. Hagimoto, T. Ishibashi and N. Shimizu, Electron. Lett. **34** (1998) 214.

[2] T. Ishibashi, N. Shimizu, S. Kodama, H. Ito, T. Nagatsuma and T. Furuta, Tech. Dig. UEO (1997) 166.

[3] T. Nagatsuma, M. Yaita, M. Shinagawa, K. Kato, A. Kozen, K. Iwatsuki and K. Suzuki, Electron. Lett. **30** (1994) 814.

[4] H. Ito, T. Furuta, S. Kodama, N. Watanabe and T. Ishibashi, Electron. Lett. **35** (1999) 1556.

[5] T. Ishibashi, H. Fushimi, T. Furuta and H. Ito, Tech. Dig. THz'99 (1999) 36.

[6] T. Furuta, H. Ito and T. Ishibashi, Extended Abst. Int. Symp. Compound Semicond. (1999) Th B1-3.

[7] T. Ishibashi, H. Ito, H. Fushimi, T. Furuta, K. Sano and N. Shimizu, Tech. Dig. CPT2000 (2000) 135.

[8] Y. Miyamoto K. Yonenaga, A. Hirano, N. Shimizu, M. Yoneyama, H. Takara, K. Noguchi and K. Tsuzuki, Tech. Dig. ECOC'98 Vol.3 (1998) 55.

[9] M. Yoneyama, Y. Miyamoto, K. Hagimoto, N. Shimizu, T. Ishibashi and K. Wakita, Electron. Lett. **34** (1998) 1607.

[10] T. Nagatsuma, N. Sahri, M. Yaita, T. Ishibashi, N. Shimizu and K. Sato, Tech. Dig. MWP'98 (1998) 5.

[11] N. Sahri, M. Shinagawa, A. Sasaki and T. Nagatsuma, Tech. Dig. CPT2000 (2000) 47.

[12] N. Sahri, T. Nagatsuma, T. Furuta, Y. Umeda and T. Ishibashi, Tech. Dig. MWP'99 (1999) 95.

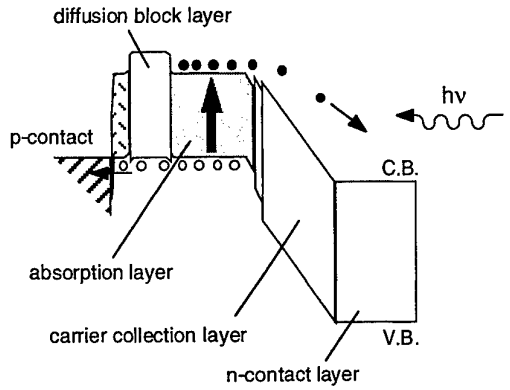

Fig. 1. Band diagram of a UTC-PD.

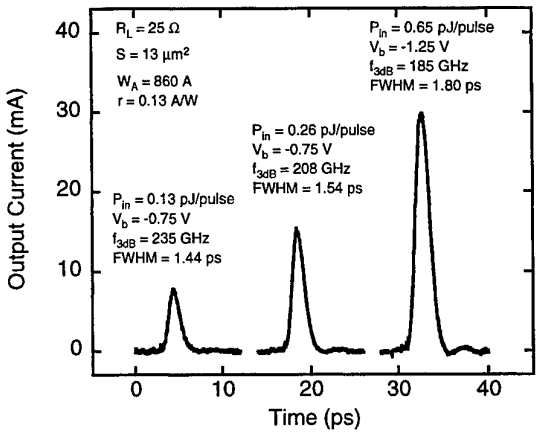

Fig. 2. Photoresponse of a high-speed UTC-PD.

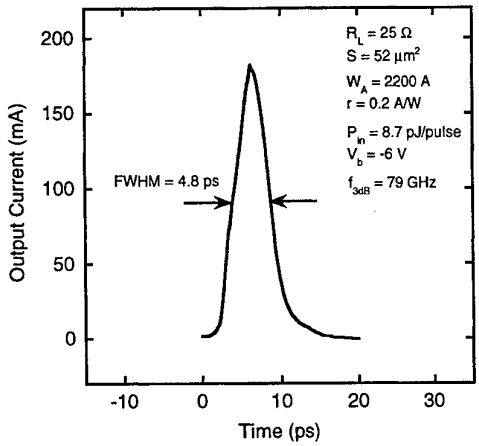

Fig. 3. Photoresponse of a high-output UTC-PD.

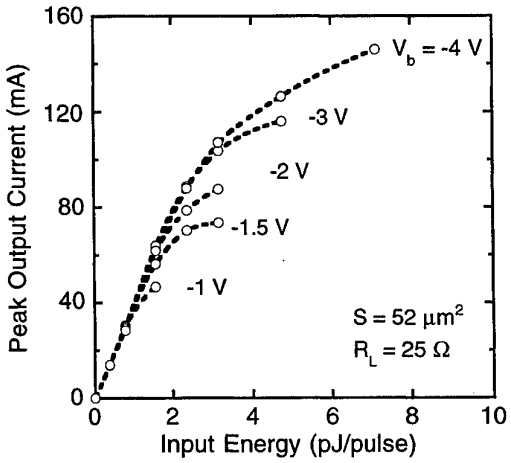

Fig. 4. Relationship between output peak voltage and pulse input energy for several bias voltages.

Internal Waveform Probing of HBT and HEMT MMIC Power Amplifiers

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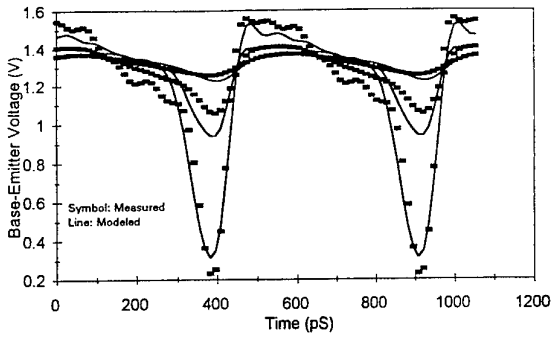
I. Introduction

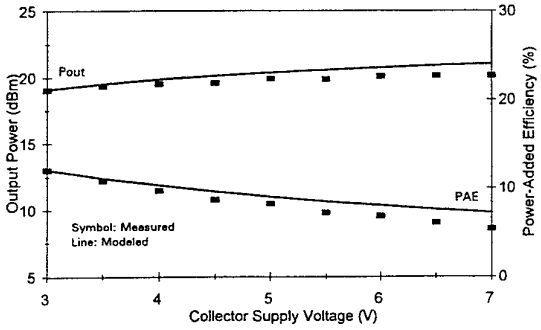
Over the last few years, with the establishment of commercial suppliers for epitaxial wafers, and the associated reduction in the cost of heterojunction materials, volume application of HBTs and HEMTs has been broadened to include monolithic microwave integrated circuits (MMICs). A number of manufacturers are now each producing several millions of HBT or HEMT MMICs every month. However, before the design of an MMIC is committed to production, ii often goes through several trial-and-error iterations that hinder the time to market the MMIC. One of the causes of such a delay is the absence of internal probing capability for design verification and diagnosis. Unlike digital or analog ICs, MMICs have been difficult to probe internally due to the lack of a broadband probe that can be conveniently applied to MMICs of standard design without perturbing their operation.

II. Experimental

Although many researchers have tried to develop an optical probe for internal probing of MMICs, for practical considerations, we have developed and used a single-contact, high-impedance probe in conjunction with a transition analyzer for MMIC internal probing [1]. Presently, both the high-impedance probe and the transition analyzer have a bandwidth of 50 GHz, which is sufficient to obtain high-fidelity time-domain waveforms on most MMICs of 10 GHz or lower—the frequency range of volume MMIC application today. The high impedance of the probe minimizes its perturbation to the MMIC under test. The single contact makes it possible to probe almost anywhere on a typical MMIC without specially designed test structures. The contact also implies that dc levels are readily obtained along with microwave signals. The transition analyzer uses a harmonic sampling technique to measure the magnitudes and phases of the harmonic components of a microwave signal. Using standard frequency-domain techniques, each harmonic as measured on the transition analyzer is corrected for instrument dispersion, before it is used to reconstruct the time-domain voltage waveform at the probe contact point. Knowing the voltage waveforms at two different probe contact points that are separated by known impedance, it is straightforward to calculate the current waveform at either contact point.



(a)



(b)

Fig. 1 Agreement between (■) measured and (—) simulated base-emitter voltage waveforms and (b) output power and efficiency of a second-stage unit cell of an HBT MMIC amplifier at 1.9 GHz. In (a), collector supply voltage = 5 V while input power = –2, 6 and 14 dBm. In (b), input power = 5 dBm.

III. Results and Discussion

Since 1994, we have used the above-described high-impedance internal probing technique to help many manufactures verify and diagnose their MMICs. Two publishable examples are illustrated below:

The first example is based on an L-band 1-W 2-stage HBT power amplifier [2]. The first stage comprises two unit cells, while the second stage comprises four unit cells. Off-chip output matching is used to reduce the chip size and power loss. On-chip active bias based on a

modified current-mirror topology is used to reduce the amplifier's sensitivity to process, temperature and power-supply variations. The first stage is biased close to Class A while the second stage is biased close to Class B.

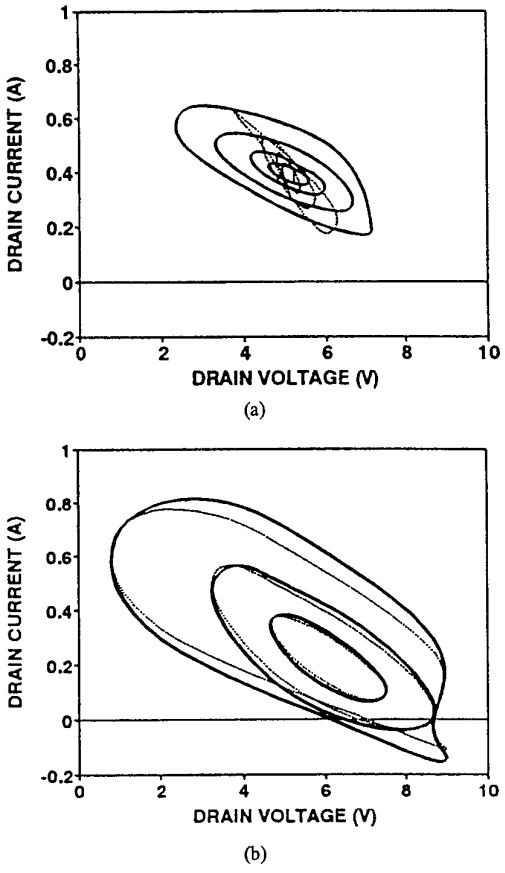


Fig. 2 Dynamic load lines of second-stage (—) inner and (—) outer unit cells measured on the (a) original and (b) redesigned HEMT MMIC amplifiers at 8 GHz. Input power = 5, 11, 17 and 23 dBm in (a) and 5, 11, 17 dBm in (b). The amplifiers were pulsed on for a period of 10 μs at a frequency of 200 Hz. The load lines were obtained from the waveform sampled at 5 μs after the amplifiers were pulsed on.

Active and passive device models were extracted and fine-tuned with the aid of measured waveforms. As the result, accurate predictions of the self-biasing and self-heating effects were achieved. Fig . 1a compares the measured and simulated voltage waveforms at the input of one of the second-stage unit cells. (All the unit cells were found to behave similarly.) It can be seen that the waveforms are clipped near the top. With increasing input power, the average base-emitter voltage decreases just as would be expected from the design of the active bias. Once agreement between measured and simulated waveforms is achieved at the unit cell level, the performance of the overall amplifier can be accurately predicted. For example, Fig. 1b confirms the predicted dependence of power and efficiency on the supply voltage.

The second example involves an X-band 5-W 2-stage HEMT power amplifier of a coplanar design [3]. The two stages of the amplifier are separately controlled through an on-chip bias- distribution network. Similar performances were obtained by either pulsing the gate supply from –6 V to 0 while maintaining the drain supply at 7 V, or by pulsing the drain supply from 0 to 7 V while maintaining the gate supply at 0. However, in either case, the performance was lower than expected.

Similar to the first example, the first stage of the amplifier comprises two unit cells while the second stage comprises four unit cells. The internal waveforms measured at the two first-stage unit cells are very similar to each other. At the second stage, the waveforms of the two inner unit cells are very similar, while that of the two outer unit cells are very similar. However, there exists a large disparity between an inner and an outer unit cell, especially at the lower edge of the band. By plotting the measured drain current waveforms vs. the measured drain voltage waveforms, Fig. 2a compares the dynamic load lines of second-stage unit cells. It can be seen that the outer unit cell is matched with too small a load that its voltage swing (hence power capacity) is more limited than that of an inner unit cell. In addition, the gain of the first stage is insufficient to drive either the inner or outer second-stage unit cell into saturation. The disparity between the inner and outer unit cells was first attributed to non-uniform processing. Once the actual design errors were uncovered and corrected, state-of-the-art performance was obtained from all unit cells (Fig. 2b) as well as the MMIC.

IV. Conclusion

A practical MMIC internal waveform probing technique has been developed. The technique can be used for model extraction, design verification, process diagnosis, and reliability assessment, as demonstrated in the above.

References

[1] C. J. Wei, Y. A. Tkachenko, J. C. M. Hwang, K. R. Smith and A. H. Peake, "Internal-node waveform analysis of MMIC power amplifiers," *IEEE Trans. Microwave Theory Techniques,* vol. 43, pp. 3037-3042, Dec. 1995.

[2] H.-C. Chung, "Modeling and characterization of HBT linear power amplifier for PCS applications using an internal node probing technique," PhD thesis, Lehigh University, 1999.

[3] J. W. Bao, C. J. Wei, J. C. M. Hwang, R. F. Wang, C. P. Wen and T. A. Midford, "On-wafer, pulsed internal-node waveform verification of improved coplanar MMIC power amplifiers," in *Dig. Int. Conf. GaAs Manufacturing Technology,* Apr. 1998, pp. 67-70.

Low-Loss Coplanar Waveguides on BCB Thin Film

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1. Introduction

During the past several years, Benzocyclobutene (BCB) has been used as an interlayer organic insulator in microwave and millimeter-wave applications. BCB has been shown to have good performance as a low-loss dielectric material in the microwave to millimeter-wave frequency range. Takahashi [1] reported on microstrip lines on BCB thin film on Si substrate having lower loss than microstrip on SiO_2 thin film on Si substrate at millimeter-wave frequencies. However there are several disadvantages with microstrip, including the dependence of the impedance on the thickness uniformity of the dielectric layer and the requirement of a ground plane under the dielectric layer, which make it difficult to realize multi-layer ICs. One solution is to use coplanar waveguides. For the first time, we have made a coplanar waveguide on a BCB layer on a Si substrate and characterized its transmission performance up to 30 GHz.

2. Experimental Results

We fabricated samples having different BCB layer thickness on both high resistivity silicon substrates (HR-Si: 380 μm thick n-type Si(100) with a resistivity of 1000 Ω-cm) and low resistivity silicon substrates (LR-Si: 650 μm thick Si(100) with a resistivity of 2-5 Ω-cm). The thickness of the lines was 5 μm, the width of the transmission line was 20 μm, and the length was 930 μm. The spacing between the transmission line and the ground line was 1 to 10 μm. The rf performance of the waveguides was characterized by measuring the S parameters in the frequency range 0.2 to 30 GHz.

Figure 1 shows the insertion loss of the coplanar waveguides on BCB/HR-Si with different BCB layer thickness. The spacing of the waveguides was 10 μm. The S_{21} parameter increases in the frequency range 0.2 to 10 GHz. The return loss (S_{11} parameter) was found to be less than -20 dB in this frequency range, but was greater than -20 dB at higher frequencies. The BCB layer on the HR-Si substrate resulted in significantly lower loss, even for the 4.8 μm BCB layer. Also, the low-loss performance did not depend on BCB layer thickness greater than 4.8 μm. Although it was reported [2] that coplanar waveguides on high resistivity silicon substrates are available for MMIC, the BCB layer showed lower loss performance even with only a 4.8 μm layer. It was also reported [3] that coplanar waveguides with V-shaped grooves on Si substrates using the micromachining technique exhibited low-loss, but the BCB layer realized low-loss coplanar waveguides without the need for the V-shaped grooves.

Figure 2 shows the dependence of the transmission performance on line spacing (1 to 10 μm) of the coplanar waveguides on 9.8 μm thick BCB/HR-Si. For the line spacing of 3 and 5 μm and transmission line width of 20 μm, the S_{11} parameter was less than -20 dB in the frequency range 0.2 to 30 GHz, and low-loss transmission was achieved. For a line spacing of 1 um, the loss increased linearly with frequency. This resulted from the high parasitic capacitance due to the narrow spacing between the transmission line and the ground line. From the standpoint of repeatability, the spacing accuracy is severe but can easily be accomplished by photolithography and electroplating technology.

Figure 3 shows the transmission performance of the coplanar line on the BCB/LR-Si in the frequency range 0.2 to 10 GHz for different BCB layer thickness. The line on the 4.8 μm thick BCB layer on LR-Si showed higher transmission loss at frequencies greater than 2 GHz, but the lines on BCB layers 9.8 μm thick and greater had low-loss performance up to 10 GHz. This indicates that BCB layer thickness greater than 10 μm on low resistivity substrates is needed to realize low-loss microwave waveguides and stable waveguide transmission characteristics.

3. Conclusions

Coplanar waveguides fabricated on BCB thin film on both high and low resistivity Si substrates have been characterized. Table 1 and 2 show the comparison of the $|S_{21}|$ of the coplanar lines. The coplanar line exhibits low-loss and good performance at microwave frequencies up to 10 GHz. Also, it shows only a small dependence on BCB thickness for thickness greater than 4.8 μm on HR-Si and greater than 9.8 μm on LR-Si. These results indicate the possibility of fabricating hetero multi-layer ICs, such as GaAs RF devices on Si ICs, by using a very simple BCB coating method and coplanar waveguides.

We will also present the results showing the rf performance of an HBT which was flip-chip bonded on the coplanar line.

4. References

[1] K. Takahashi, T. Yoshida, and H. Sakai, "Millimeter-Wave Circuit Technology Applying Flip-Chip Bonding,"

1996 Microwave Workshops and Exhibition Digest, Yokohama, Japan, pp. 180-185, December 10-12, 1996.
[2] W. Heinrich, J. Gerdes, F. J. Schmuckle, C. Rheinfelder, and K. Strohm, "Coplanar Passive Elements on Si Substrate for Frequencies up to 110 GHz," IEEE Trans. on Microwave Theory and Techniques, vol. 46, No.5, pp. 709-712, May 1998.
[3] K. J. Herrick, T. A. Schwarz, and L. P. B. Katchi, "Si-Micromachined Coplanar Waveguides for Use in High-Frequency Circuits," IEEE Trans. on Microwave Theory and Techniques, vol. 46, No. 6, pp. 762-768, June 1998.

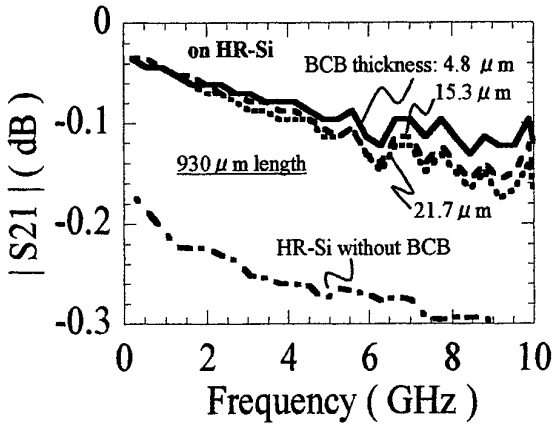

Fig. 1. S_{21} parameter of the coplanar waveguide on BCB/HR-Si substrate with different BCB layer thickness.

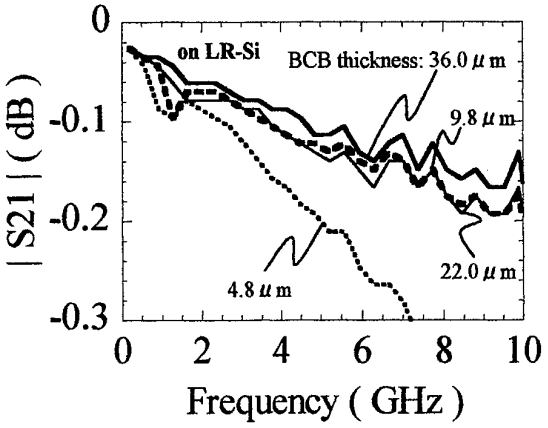

Fig. 3. S_{21} parameter of the coplanar waveguide on BCB/LR-Si substrate with different BCB layer thickness.

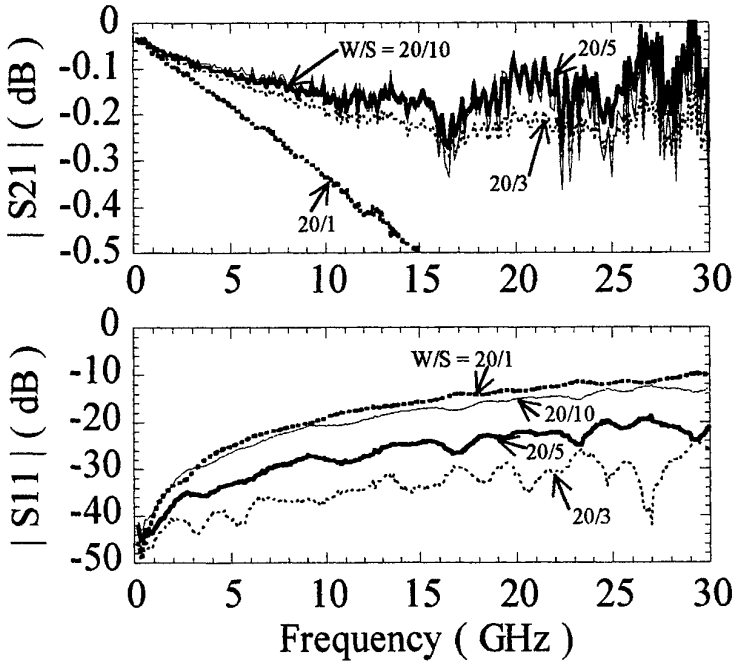

Fig. 2. S21 and S11 parameters of coplanar waveguides with different spacing on BCB/HR-Si substrate. The BCB thickness is 9.8 μm. The transmission line width (W) and length are 20 μm and 930 μm, respectively. The spacing (S) varies between 1 and 10 μm.

Table 1. Comparison of |S21| parameter

Substrate	BCB thickness (μm)	|S21| (dB) @ 5GHz	@ 10GHz
HR-Si	0	-0.264	-0.317
	4.8	-0.096	-0.167
	15.3	-0.114	-0.211
	21.7	-0.114	-0.228
LR-Si	4.8	-0.211	-0.501
	9.8	-0.131	-0.247
	22.0	-0.140	-0.247
	36.0	-0.114	-0.229

Table 2. Comparison of |S21| parameter

Substrate	line(μm) / spacing(μm)	|S21| (dB) @ 5GHz	@ 10GHz
HR-Si*	20/ 1	-0.184	-0.337
	20/ 3	-0.122	-0.202
	20/ 5	-0.105	-0.175
	20/ 8	-0.096	-0.167
	20/10	-0.096	-0.175

*BCB thickness is 9.8 μm

Terahertz Photon-Assisted Tunneling in Resonant Tunneling Diode Integrated with Patch Antenna

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We report current change under THz irradiation in triple-barrier resonant tunneling diodes (RTDs) due to photon-assisted tunneling (PAT). By using patch antennas with low conduction loss, large THz voltage was induced across the RTDs. Electron transition with multi-photon process was observed, and good agreement between theory and measurement was obtained.

The interaction between THz electromagnetic waves and nanostructures has received considerable attention[1][2]. A three-terminal THz amplifier device using PAT has also been proposed[3]. We previously reported small current change in RTDs by THz irradiation including gradual change from square-law detection to PAT with increasing frequency[4]. In this paper, we report the THz PAT of triple-barrier RTDs including large current changes by using patch antennas with low conduction loss. Electron transition with multi-photon process was observed due to large THz voltages.

GaInAs/InAlAs triple-barrier RTDs on n^+-InP substrates integrated with planar patch antennas were used for the THz detection, as shown in Fig.1 (a) and (b). To reduce the conduction loss of the antenna due to the skin effect, the substrate was coverd with Au and a large antenna cavity was constructed with 3μm-thick benzo-cyclo-butane (BCB).

Figure 2 shows measured I-V characteristics under the irradiation for different THz voltages V_{ac} across the diode. Theoretical curves taken into account the multi-photon process in Fig.3 agree semi-quantitatively with the measurement. The multi-peak shape as in [2] was not observed because the peak width of the measured I-V characteristics is larger than $\alpha\hbar\omega/e$, where α is the ratio of the bias voltage to the applied voltage between the wells[4]. The voltage interval between the left-side peak under irradiation and the peak without irradiation was plotted as a function of $V_{\rm ac}$, as shown in Fig.4. The values of $eV_{\rm ac}/\alpha\hbar\omega$, which roughly implies the dominant photon number in the multi-photon process, are also indicated on the horizontal axis of Fig.4. When $eV_{\rm ac}/\alpha\hbar\omega$ is around 1 (one-photon process), the voltage interval is almost constant. With increasing $eV_{\rm ac}/\alpha\hbar\omega$, the multi-photon process appears, and the voltage interval becomes large. The measurement and calculation are in good agreement. The square root of the reduction of the straight resonant tunneling current, $\Delta I^{1/2}$, is shown in Fig.5 as a function of $eV_{\rm ac}/\alpha\hbar\omega$ for different irradiation frequencies. With increasing $V_{\rm ac}$, $\Delta I^{1/2}$ saturated due to multi-photon process. The curves as a function of $V_{ac}/\alpha\hbar\omega$ in Fig.5 are almost independent of frequency, indicating that the multi-photon process arises more easily in lower frequencies.

[1] T.C.L.G. Sollner, W.D. Goodhue, P.E. Tannenwald, C.D. Parker and D.D. Peck, Appl. Phys. Lett. **43**(1983)588.
[2] H. Drexler, J.S. Scott, S.J. Allen, K.L. Campman and A.C. Gossard Appl. Phys. Lett. **67**(1995)2816.
[3] M.Asada, Japan.J.Appl.Phys., **35** (1996) L685
[4] Y. Oguma, N. Sashinaka, M. Asada,Jpn. J. Appl. Phys. **38**(1999)L717.

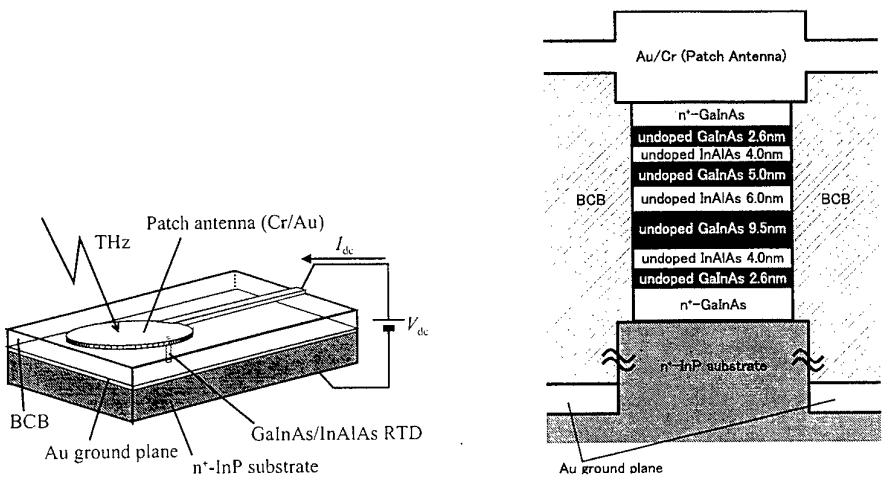

Fig.1 (a)RTD intergrated with a THz patch antenna used for the measurement of photon-assisted tunneling. (b)Cross-section of the diode buried benzo-cyclo-butane(BCB) layer of the antenna.

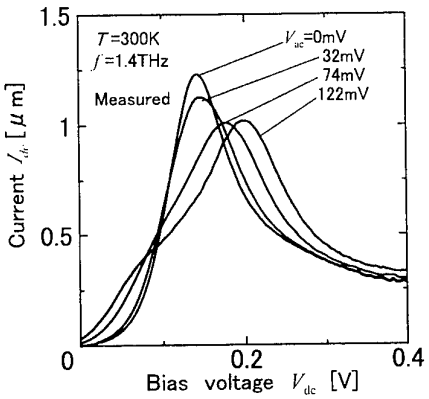

Fig.2 Measured *I-V* curves under THz irradiation.

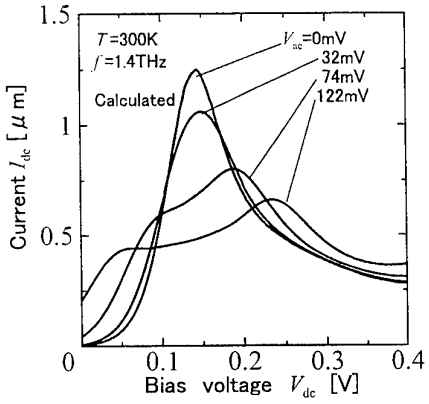

Fig.3 Calcualted *I-V* curves under THz irradiation.

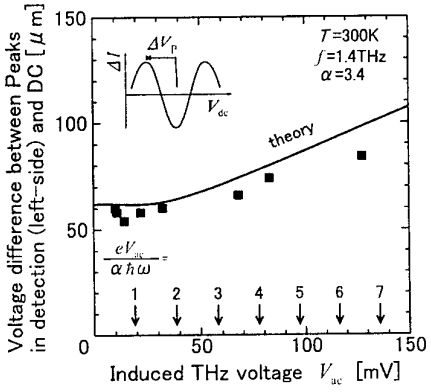

Fig.4 Voltage interval between the left-side peak under irradiation and the peak without irradiation, as a function of THz voltage induced across the RTD.

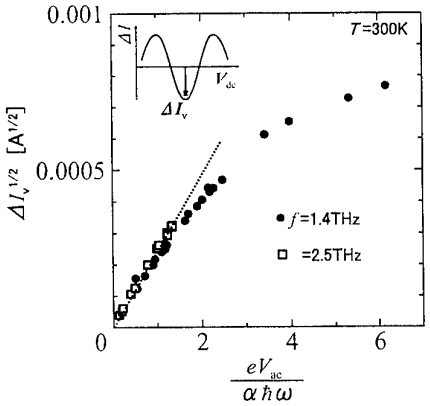

Fig.5 Square root of the reduction of the straight resonant tunneling current as a function of THz voltage across the RTD for different irradiation frequencies.

Plasma-Wave Transistors with Virtual Carrier Excitation Using Polariton-Plasmon Coupling for Terahertz Applications

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Emerging information technologies necessitate further extension of operating frequency bands in electronic systems to beyond terahertz (THz). Conventional semiconductor device technologies, which rely upon real-carrier transport, however, face to the substantial limit of operation in the THz region. New operating principles should be appreciated to establish novel THz device technology for the real applications.

In terms of flexible, high capacity, future optical network systems, coherent heterodyne detection utilizing THz IF bands will be a unique, possible solution. Fig. 1 shows the newly proposed conceptual system block diagram. Fundamental key devices are (1) quasi-optic broadband mixers that generate a replica of the WDM optically-coded data in the THz IF band by photomixing the optical data with the subcarrier, (2) tunable injection-locked CW THz oscillators, and (3) THz mixers that transfer the IF signal of one target channel into the baseband. In this system, real-time, adaptive wavelength routing for add-drop multiplexing can be performed in a manner of mixed electrical and quasi-optical signal processing.

Two-dimensional electron plasma in the electron channel of submicron FET's can make resonant oscillation in the THz range. Fig. 2 shows a schematic of the plasma oscillation in the channel. Dyakonov and Shur formulated the 2-D plasma dynamics as a function of device parameters and applied bias voltages [1]. The THz radiation can be coherently absorbed via inter-subband transitions of conduction electrons if the electrons are transversely well confined in the channel. The resonant intensity increases with the plasma coherency, or equivalently with $v_p\tau/L$, where v_p the plasma-wave velocity, τ the momentum relaxation time of electrons, L the gate length. The condition, $v_p\tau/L=1$, gives the break-even point for the resonance where the plasma coherence length corresponds to the gate length. The resonance frequency is given by the standing-wave condition, and is proportional to v_p/L. The resonant conditions can be externally controlled by the gate bias potential V_g, since v_p is proportional to the square root of V_g when the drain bias is negligibly small. This offers the tunability of oscillation.

The plasma-wave transistors can configure the injection-locked CW THz oscillators needed in the optical network systems shown in Fig. 1. One alternative to attaining coherent THz IF-signal detection is the direct photomixing, which needs a mean of coherent plasma excitation by the beat frequency component of photomixing 1.55-μm optical signals. Photo-excited real carriers violate the coherency because of their long relaxation time. Virtual carrier excitation with photon energies lower than the bandgap (E_g) of the channel will be a solution. Hirakawa et al. experimentally suggested that the photon with $<E_g$ coherently couples with the plasmon via polariton [2]. In case of InGaAs/InAlAs/InP HEMTs, the bandgap of the InGaAs channel must be greater than the photon energy of incoming 1.55-μm signals. The pseudomorphic structure with an In composition of <45% meets this requirement.

Fig. 3 plots the simulated plasma resonant intensity at 300 K and a 1-V V_g for typical three types of FET devices, InGaAs/InAlAs/InP HEMT, GaAs MESFET, and Si MOSFET as a function of the gate length. The scattering factors considered are the phonon, the ionized impurity, and the vertical electric field. The electron-electron scattering was assumed to be weaker than the electron-phonon scattering by orders. 0.1-μm-class InP-based HEMTs exhibit the highest resonant intensity due to their excellent electron transport property. The dependence of the resonance frequency on V_g was simulated for a 30-nm gate-length InP-based HEMT (Fig. 4). The resonance-intensive regions ($v_p\tau/L > 5$) are specified with thick lines. The result indicates its potential wide operating range from THz to >100 THz. The validity of the proposed device and system is to be verified experimentally.

Acknowledgment: The authors appreciate valuable discussion with K. Narahara and E. Sano of NTT, and with Prof. T. Asano. This work was partly supported by NTT Network Innovation Laboratories.

References
[1] M. Dyakonov and M.S. Shur, IEEE Trans. Electron Device, **43-3**, 380 (1996).
[2] K. Hirakawa, et al., IEEE Int. Conf. Terahertz Electron. Proc., 109 (1999).

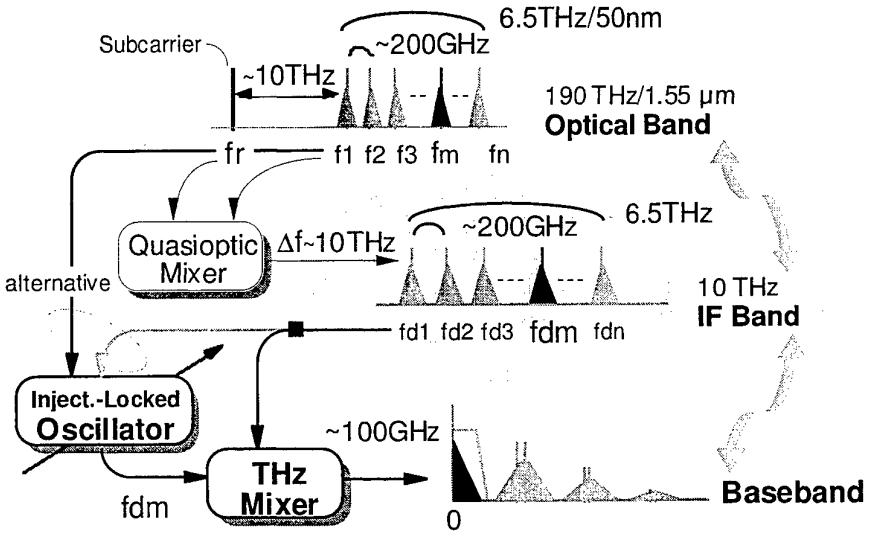
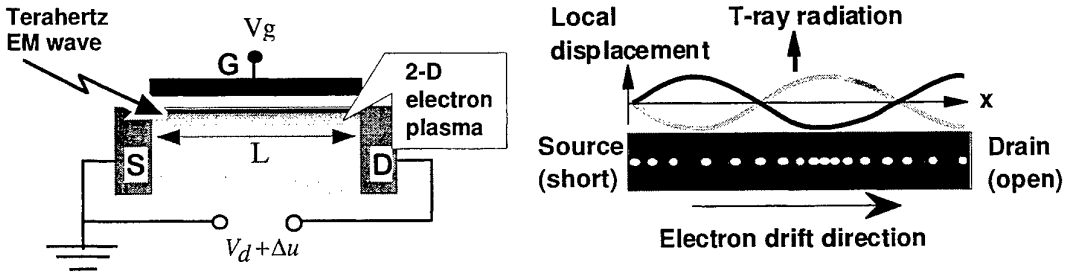


Fig. 1. Real-time adaptive wavelength routing utilizing coherent heterodyne detection via THz IF band for future optical network systems.



(a) (b)

Fig. 2. Plasma-wave transistor. (a) device cross section, (b) plasma resonance in the channel.

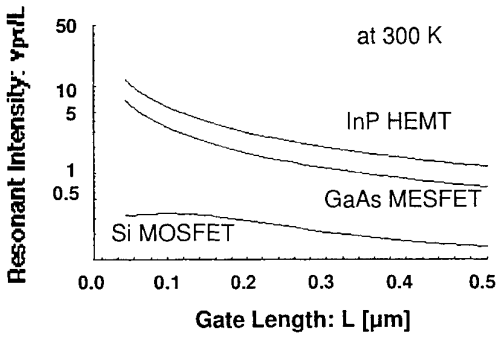


Fig. 3. Simulated plasma resonant intensity vs. gate length for three types of FET's at 300 K and a gate bias of 1.0 V.

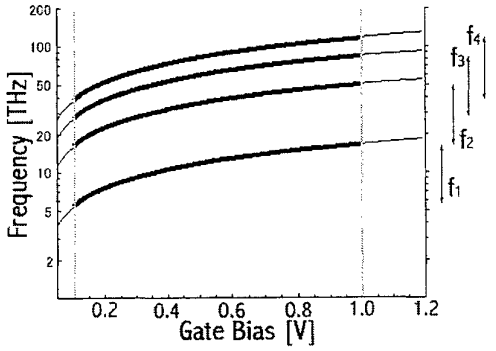


Fig. 4. Simulated plasma resonance frequency vs. gate bias voltage. fn (n = 1~4): the fundamental (n = 1) and harmonic oscillations.

Analytical expression of maximum bias slew rate of RTD-pair circuit

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High-speed circuits including RTDs(resonat-tunneling diodes) are attracting attention recently, because of their potential of overcoming the speed limitation of conventional circuits [1]. An RTD-pair circuit is capable of the latching and high-speed operation and makes the best use of the characteristics of RTDs [2, 3]. Sollner et al. [4] obtained an expression for the maximum clock slew rate, which is determined by the peak current difference and the capacitance of the driver RTD. This expression gives an operation speed of the RTD-pair circuit that is much lower than the speed given by the speed factor of an RTD, j_p/C, when the peak current difference is small. Maezawa[5] showed by SPICE simulation that the RTD-pair circuit can operate much faster than the estimate given by Sollner et al. However, there has not been any figure of merit that quantitatively describes the speed limitation of the RTD-pair circuit because of its intrinsic multistable nature.

In this paper, we propose a novel graphical method which well describes the multistable nature of RTD-pair circuits. Using this method, we obtained the analytical expression of a key factor that limits the bias slew rate when bias voltage is raised. Our results quantitatively match the results of SPICE simulation, which used a realistic RTD SPICE model.

We analyze the RTD-pair circuit depicted in Fig. 1(a). H stands for any device which is used to control the current flowing through the node between the two RTDs. H can be an FET [2] or PD [3], and can also include the effect of the devices connected to the output terminal. H is considered to be a capacitor, in order to analyze the circuit's operation when FET or PD is totally depleted. In the equivalent circuit shown in Fig. 1(b), C_0 corresponds to the capacitor that is associated with FET or PD, and also include the effects of the capacitors of the subsequent stages. The time evolution of the circuit's state (V_{bias},V_1) is governed by the following current continuity equation,

$$C_U \frac{d(V_{bias}-V_1)}{dt} + i_{D2}(V_{bias}-V_1) = C_D \frac{dV_1}{dt} + i_{D1}(V_1). \quad (1)$$

Now we can plot the contour diagram of the current ΔI which charges the capacitors (Fig. 2),

$$\Delta I\,(V_{bias},V_1) = i_{D2}(V_{bias}-V_1)-i_{D1}(V_1) \quad (2)$$

In Fig. 2, the peak currents of RTDs D1 and D2 are defined to be 4 mA and 8 mA, respectively. The contour diagram well describes the multistable nature of the RTD-pair circuit and can be used to analyze its time evolution. When the bias slew rate dV_{bias}/dt is small (quasi-static operation), the circuit should evolve on the equilibrium line, which satisfies ΔI =0 and the stability condition(thick solid lines). From the figure, we can see that the circuit's state evolves from V_1=0 V to V_1=0.77 V, when V_{bias} is raised from 0 to 0.8 V, following thick solid lines with a small jump at V_{bias}=0.48 V. This is the correct "HIGH" operation of an RTD-pair circuit when the driver RTD (D1) has a smaller peak current than the load RTD (D2).

When dV_{bias}/dt is not negligible, the circuit's state does not stay on the equilibrium line. The RTD-pair circuit can evolve to an incorrect "LOW" state when the slew rate of V_{bias}, (dV_{bias}/dt) exceeds some certain threshold. The threshold can be quantified by using the contour diagram to analyze the circuit's evolution . The SPICE simulation results along with the contour diagram in Figs. 3 and 4 suggest that the saddle point $(2V_P,V_P)$ is the critical point that determines the threshold. We obtained the necessary condition for correct operation that the slope of the velocity vector $(dV_{bias}/dt, dV_1/dt)$ is larger than the slope α of the contour at the saddle point in Fig. 4. Using eq. (1), the condition is written as

$$\frac{dV_1/dt}{dV_{bias}/dt} = \frac{C_U}{C_U+C_D} + \frac{\Delta I}{(C_U+C_D)dV_{bias}/dt} > \alpha \quad (3)$$

It leads to the following condition, which defines the analytical form of the maximum bias slew rate (MBSR),

$$\frac{dV_{bias}}{dt} < \frac{\Delta I_P}{\alpha C_D - (1-\alpha)C_U} \quad (4)$$

Using a linear approximation, α is expressed as $I_{pD2}/(I_{pD1}+I_{pD2})$, where I_{pD1} and I_{pD2} are the peak currents of the D1 and D2, respectively. In the present case, α=0.67. Figure 5 plots the MBSR given by the right-hand-side of (4) against C_0. Its agreement with the SPICE simulation result is much better than the simple estimation of $dV_{bias}/dt<\Delta I/C_D$ [4], which corresponds to α=1 in (4).

Consequently, our results suggest that the slew rate when bias voltage is raised can be made large even for a small peak current difference, when the capacitors are properly designed. In such a case, the speed limitation of the RTD-pair circuit is primally governed by the difference of the peak and the valley current, and not by difference in peak currents of the two RTDs.

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References: [1] A. Seabaugh et al., IEEE Proc. of IEDM, pp. 429-432, (1998). [2] K. Maezawa et al., IEEE EDL, **19**, pp. 80-82 (1998). [3] K. Sano et al., Electron. Lett., **35**, pp. 1376-1377 (1999). [4] Sollner et al., Int. Semicond. Devices. Res. Symp., Charlettesville, 307 (1993) [5] K. Maezawa, Jpn. J. Appl. Phys. **34**, 1213 (1995).

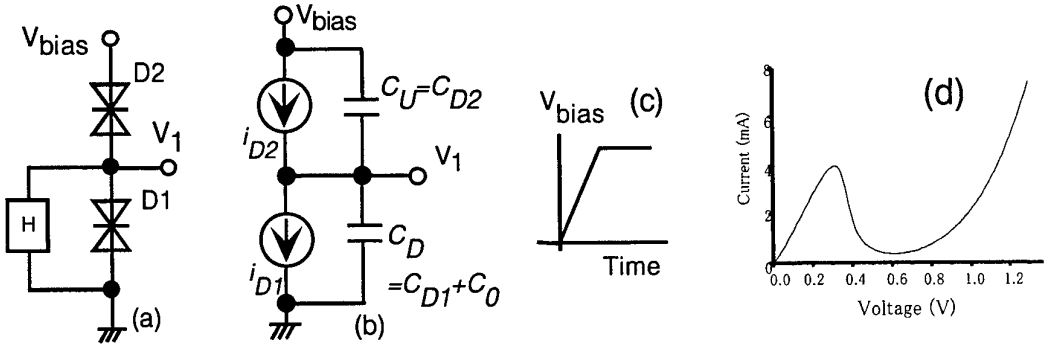

Fig. 1. (a) RTD-pair circuit, (b) its equivalent circuit, (c) time dependence of V_{bias} and (d) I-V characteristic of RTD D1.

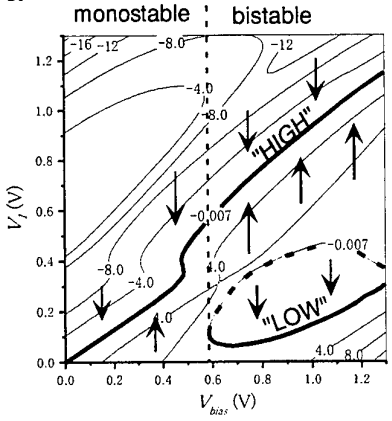

Fig. 2. Contour diagram of the current ΔI which charges capacitors.

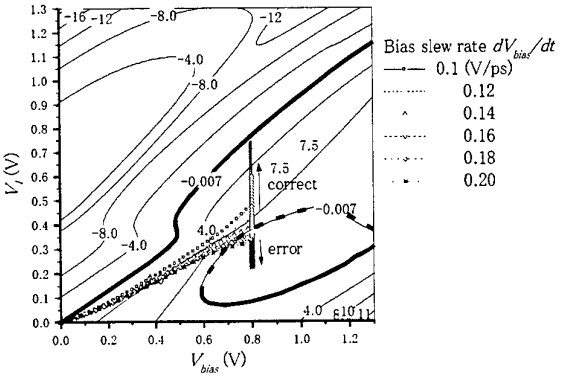

Fig. 3. Evolution of the circuit's state in the clock-up phase on the contour diagram.

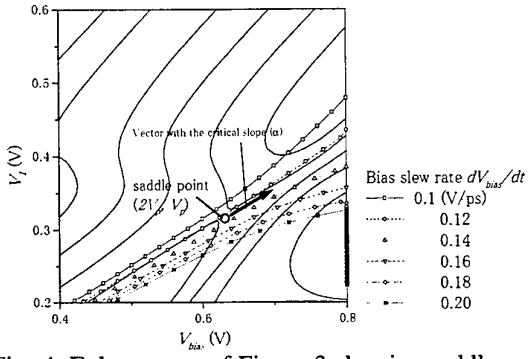

Fig. 4. Enlargement of Figure 3 showing saddle point and critical slope.

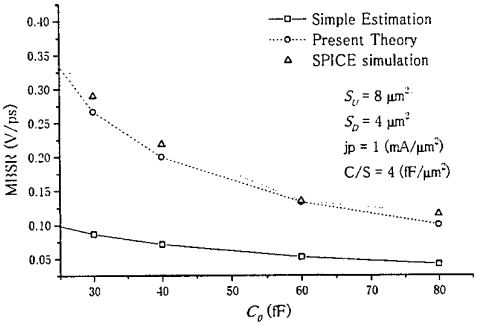

Fig. 5. Maximum bias slew rate (MBSR) versus C_0.

GaAs Double Heterojunction Bipolar Transistors with a Pseudomorphic GaAsSb Base

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GaAs-based heterojunction bipolar transistors (HBTs) have demonstrated excellent high-frequency performance, and have attracted considerable attention as key devices in high-speed applications such as 10-40 Gb/s optical transmission systems and microwave/millimeter-wave wireless communication systems. However, the turn-on voltage is relatively large owing to the large bandgap energy of GaAs used as the base layer, and this increases power consumption in integrated circuits and limits the minimum operating voltage. Although low-voltage operation is achieved by using Si bipolar transistors or InP-based HBTs, these devices have certain disadvantages compared to GaAs HBTs: low breakdown voltages for both devices, lack of semi-insulating substrates for Si, and less mature process technology for InP. Therefore, we focused on decreasing the turn-on voltage in GaAs HBTs by using GaAsSb as the base layer. GaAsSb has a definite advantage over InGaAs; i.e., the bandgap difference between GaAs and GaAsSb appears predominantly across the valence band [1]. This suggests that the conduction band discontinuity is extremely small, thus we can avoid inserting graded layers at the heterojunction interfaces and can simplify the epitaxial growth procedures. Furthermore, base contact resistance can be decreased because of the small potential-barrier height at the metal/*p*-GaAsSb interface [2], which will lead to potentially faster devices. In this paper, we demonstrate GaAs DHBTs with a pseudomorphic, fully-strained GaAsSb base.

The epitaxial layers were grown by MBE using Si and Be as *n*- and *p*-type dopants, respectively. The Sb content x of $GaAs_{1-x}Sb_x$ base layer was 0.1, and the critical thickness of the layer was calculated to be 307 Å [3]. The *n*-GaAs subcollector layer was 3500 Å thick and doped to 5×10^{18} cm^{-3}. The GaAs collector layer was 1500 Å thick and undoped. The *p*-$GaAs_{0.9}Sb_{0.1}$ base layer was 280 Å thick and doped to 2×10^{19} cm^{-3}. A 20 Å undoped $GaAs_{0.9}Sb_{0.1}$ spacer layer was inserted between the base and the emitter layers to prevent the shift of the *p-n* junction towards the emitter layer due to Be diffusion. The total $GaAs_{0.9}Sb_{0.1}$ thickness was below the critical thickness. The emitter layer was 500 Å thick *n*-GaAs doped to 1×10^{18} cm^{-3}. Highly doped *n*-GaAs (1000 Å, $n = 5 \times 10^{18}$ cm^{-3}) and *n*-$In_{0.5}Ga_{0.5}As$ (500 Å, $n = 4 \times 10^{19}$ cm^{-3}) emitter-cap layers were grown on the emitter layer. Mesa structure devices were fabricated by using wet chemical etching and a standard photolithographic process. Figure 1 shows a transmission electron microscopy (TEM) cross section of the GaAs/$GaAs_{0.9}Sb_{0.1}$/GaAs DHBT epitaxial layers. No misfit dislocations were observed in the $GaAs_{0.9}Sb_{0.1}$ layer. We observed the surface morphology of the epitaxial wafer by Nomarski interference contrast microscopy, but no cross-hatched patterns were observed, either. These results suggest that the $GaAs_{0.9}Sb_{0.1}$ base layer is fully strained.

Figure 2 shows the dependence of the collector current density J_C on the emitter-base bias voltage V_{BE} of the fabricated GaAs/GaAsSb DHBT and an InGaP/GaAs HBT grown by gas-source MBE [4]. The turn-on voltage of the GaAs/$GaAs_{0.9}Sb_{0.1}$ DHBT was reduced by 0.10 V compared to that of the InGaP/GaAs HBT. Figure 3 shows the common-emitter $I_C - V_{CE}$ characteristics of the fabricated DHBT with an emitter-base junction area S_{EB} of 3.5×5.5 μm^2. The current gain h_{fe} reached 25 at J_C of 8×10^4 A/cm^2, and the low knee voltage of 0.48 V was attained at J_C of 5×10^4 A/cm^2. We attribute these characteristics under high-current density operation to the suppression of the collector current blocking effect due to the extremely small conduction band discontinuity. The offset voltage was about 0.1 V, which is relatively large despite the near potential symmetry of the DHBT. In contrast, we obtained a small offset voltage of about 0.04 V for a DHBT with S_{EB} of 20×50 μm^2. The larger offset voltage for the smaller device is probably due to the relatively large area of the base-collector junction caused by the non-self-aligning process, which leads to the large forward current at the base-collector junction (I_{BC}) compared to the forward current at the emitter-base junction (I_{EB}). We thus believe that the offset voltage can be further reduced by using a self-aligning process. Figure 4 shows the specific contact resistance ρ_C of *p*-$GaAs_{0.9}Sb_{0.1}$ and *p*-GaAs as a function of carrier concentration P_B. The ρ_C of *p*-$GaAs_{0.9}Sb_{0.1}$ was 8×10^{-7} $\Omega \cdot cm^2$ at the relatively low doping level of

2×10^{19} cm^{-3}. The Schottky-barrier height ϕ_B of p-$GaAs_{0.9}Sb_{0.1}$ was estimated to be about 0.15 eV lower than that of p-GaAs. This result implies that GaAsSb can reduce the base resistance and thus improve high-frequency characteristics.

In summary, we have developed GaAs/GaAsSb/GaAs DHBTs with low turn-on voltage, low knee voltage, and low base contact resistance, demonstrating the feasibility of GaAs DHBTs with a pseudomorphic GaAsSb base.

REFERENCES

[1] L. Esaki, *J. Crystal Growth*, vol. 52, pp. 227-240, 1981.
[2] J. –I. Chyi et al., *Appl. Phys. Lett.*, vol. 55, pp. 570-571, 1989.
[3] R. E. Nahory et al., *J. Appl. Phys.*, vol. 48, pp. 1607-1614, 1977.
[4] K. Ouchi et al., *Japan. J. Appl. Phys.*, vol. 36, pp. 1866-1868, 1997.

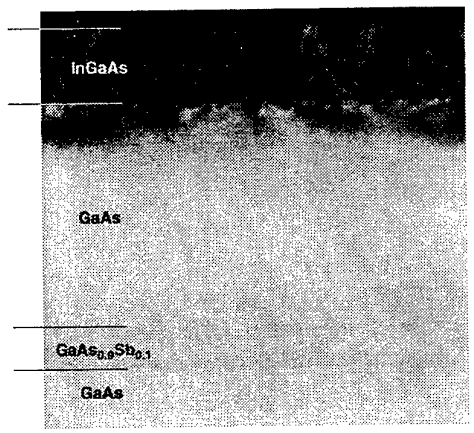

Fig. 1. TEM cross section of GaAs/GaAsSb/GaAs DHBT epitaxial layers.

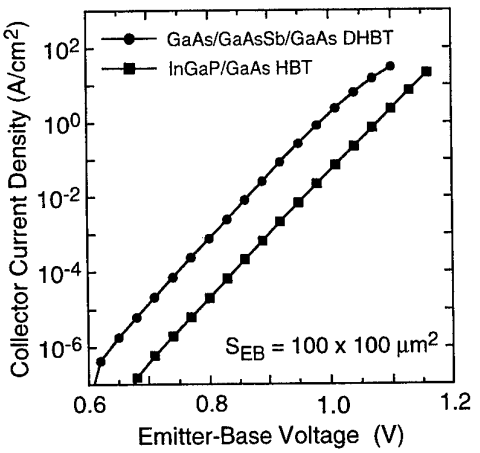

Fig. 2. The dependence of collector current density on emitter-base bias voltage of the fabricated GaAs/GaAsSb/GaAs DHBT and an InGaP/GaAs HBT grown by gas-source MBE.

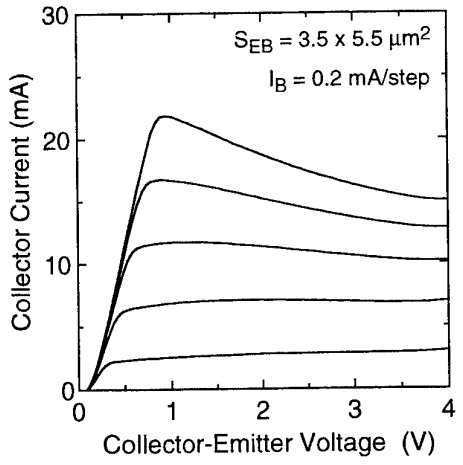

Fig. 3. Common-emitter *I-V* characteristics of fabricated DHBT with an emitter-base junction area of 3.5 x 5.5 μm^2.

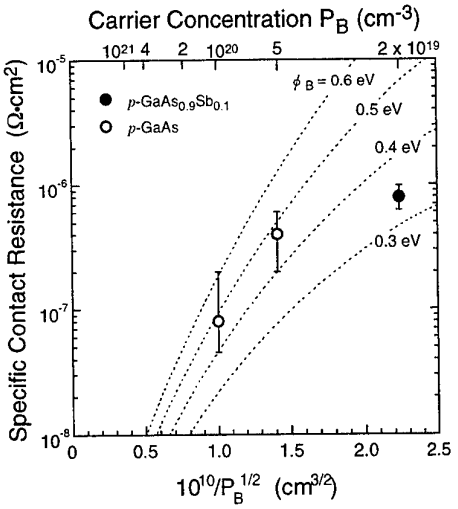

Fig. 4. The specific contact resistance of p-GaAsSb and p-GaAs as a function of carrier concentration P_B.

Emitter interface in InP-based HBTs with InAlAs/InP composite emitters

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One approach to reducing the recombination on the surface of the extrinsic base of an HBT is to leave a thin depleted layer of the emitter on the base [1]. Processing is simplified in this approach if the emitter is made from two materials, for which selective etches are known. This idea of a composite emitter has been proposed [2] and used [3] for AlGaAs/GaInP emitters, and for InP/InAlAs HBTs with quaternary materials in the emitter [4].

A composite emitter can combine benefits of both layers. In a composite emitter of AlGaAs/InGaP, for example, the InGaP blocks holes from the base, and the AlGaAs, with a larger discontinuity in the conduction band, injects energetic electrons through the InGaP into the base [2]. A similar combination is possible in InP-based HBTs, using InP to block the holes and InAlAs to inject energetic electrons. We report on this combination of InP and InAlAs here, for a series of HBTs with different thicknesses of InP.

The layers were grown by MBE at 425°C; the relatively low growth temperature prevents diffusion of Be. Dipole doping was used to reduce the blocking from the barrier in the collector [5]. Seven emitter structures were studied: five composite emitters with 75 nm InAlAs and InP thicknesses of 5 nm, 10 nm, 15 nm, 20 nm, and 40 nm; and two reference structures, one with a 75-nm InAlAs emitter, the other with a 90-nm InP emitter.

For all but the thickest InP layers, the collector currents in the Gummel plots are controlled by the height of the InAlAs barrier. As the InP thickness increases, both the collector current $I_c(V_{BE})$ at a given bias and the ideality factor of the collector current increase, as expected from Ebers-Moll models [6]. The gain is higher for thinner InP layers, consistent with the increase in injection energy of electrons. At low bias, the gain is lowest for reference samples with simple InP or InAlAs emitters, because these have no thin passivating layer on the base.

If the InAlAs/InP interface is identical between samples, then the ratio of currents between two samples at a given bias is $I_2/I_1 = \exp(q F_{eff} \delta a/kT)$, where δa is the difference in thickness of the InP layers between the two samples, and F_{eff} is the electric field at the interface. The effective field estimated in this way is almost a factor of three smaller than the field expected from the emitter doping; both SIMS and capacitance measurements, however, confirm that the emitter doping is 2-3×10^{17} cm^{-3}, as specified in the growth conditions. The anomalously small value of F_{eff} indicates that F_{eff} is not the actual field, and so we conclude that the InAlAs/InP interface is not identical between samples. Thus increasing the thickness of InP changes the InAlAs/InP interface in some systematic way, so that the interface appears to become more abrupt as the thickness of InP increases.

[1] R.J. Malik et al, Electronics Letters 25, 1175-7 (1989).
[2] J. Hu et al, IEEE Electron Device Letters 14, pp. 563-5 (1993).
[3] J.-W. Park et al, Proc. IEEE 24th Int. Symp. Compound Semicond., 439-42 (1998).
[4] R.N. Nottenburg et al, Elec. Dev. Lett. 8, 282-4 (1987).
[5] S.P. McAlister et al, J. of Appl. Phys. 82, 5231-4 (1997).
[6] M.S. Lundstrom, Solid State Electronics 29, 1173-9 (1986).

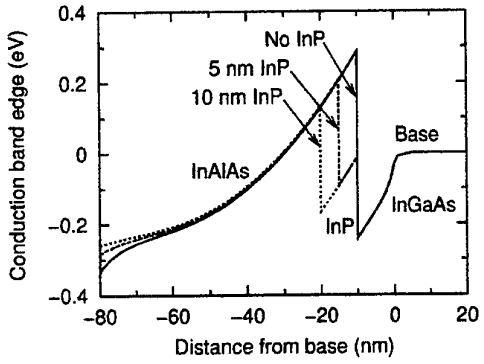

Fig. 1. Conduction band edge calculated from drift-diffusion simulations for three thicknesses of InP, at a base-emitter voltage of 0.5 V. As the InP thickness increases, the barrier to electrons decreases.

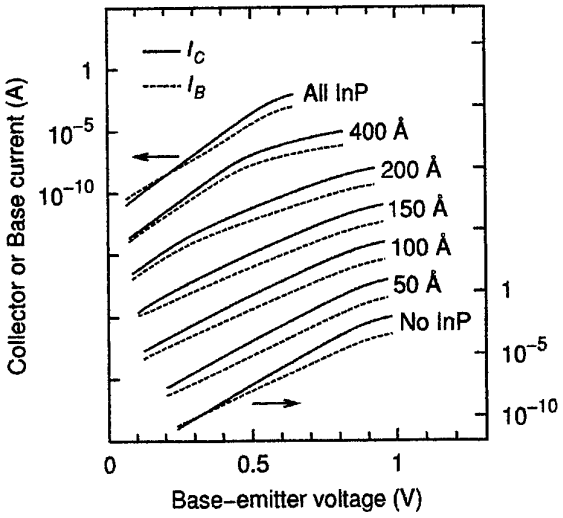

Fig. 2. Gummel plots for the series of seven emitter structures, with thickness of the InP layer indicated, for HBTs with emitter areas of 50×50 μm^2. Each subsequent pair of I_b and I_c curves is shifted down by 1000; the top pair of curves (all InP) corresponds to the vertical scale on the left, and the bottom pair to the vertical scale on the right.

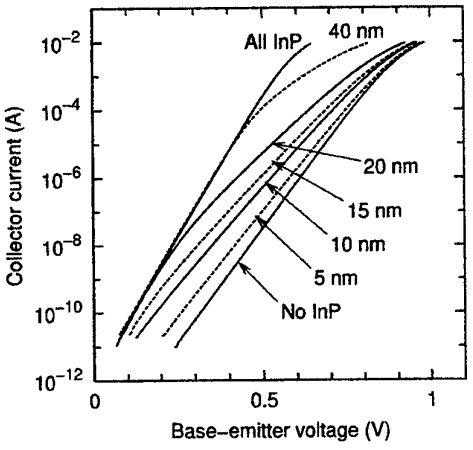

Fig. 3. Collector currents from the Gummel plots in Fig. 2. An effective electric field in the emitter can be calculated from the roughly equal spacing between the curves for thinner InP layers.

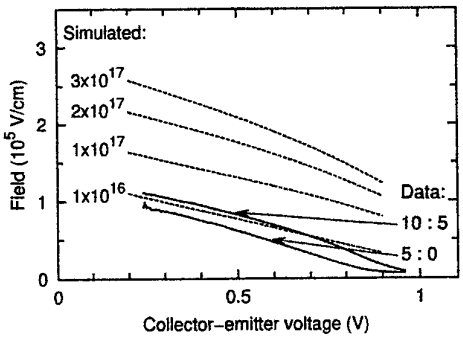

Fig. 4. Effective electric field at the InAlAs/InP interface calculated from the ratio of collector currents for devices of 10 nm and 5 nm, and 5 nm and 0 nm, and electric field at the interface calculated from the depletion approximation for four emitter dopings from 1×10^{16} to 1×10^{17} cm^{-3}.

InP DHBT with 0.5 μm wide emitter along <010> direction toward BM-HBT with narrow emitter

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Abstract

Fabrication process for narrow emitter along <010> direction in heterojunction bipolar transistor fully drawn by EB-lithography was studied. Emitter structure of 100 nm width was formed by using 30-nm-thick InP layer. Transistor operation of devices with 0.5-μm-wide emitter was confirmed. This process could be applied to buried metal heterojunction bipolar transistor with narrow emitter.

Introduction

In heterojunction bipolar transistors (HBTs), reduction of total base-collector capacitance (C_{BCT}) is effective in the improvement of high speed operation. We proposed buried metal heterojunction bipolar transistor (BM-HBT), in which tungsten stripe with a same area of emitter is buried by InP collector layer and it could reduce C_{BCT} [1]. Reduction of C_{BCT} was demonstrated by BM-HBT with emitter width of 2 μm [2]. Calculated dependence on emitter width shows that maximum oscillation frequency (f_{MAX}) can be increased with decrease of emitter width without penalty of current gain cutoff frequency (f_T). Thus, fabrication process for BM-HBT with narrower emitter is attractive. For buried growth of tungsten stripe, emitter mesa must be along <010> direction [3]. In case of this direction, undercut etching of InP can not be stopped. Thus, reduction of emitter size have difficulty in control of undercut etching. In this report, fabrication process with 100-nm-wide emitter along with <010> direction and fabrication of conventional HBT with 500-nm-wide emitter along <010> direction are described.

To control undercut etching, thinner InP layer as the emitter was preferable. So, five HBTs structure with different thickness of InP layer were fabricated on (100) InP substrate. Table 1 shows epitaxial layers of HBT grown by organometallic vapor phase epitaxy. Figure 1 shows the current gain of HBT with emitter mesa area of 50×50 μm^2 as a function of InP layer thickness. When emitter thickness was less than 30 nm, current gain decreased. However, current gain of 50 could be obtained when total InP thickness was 20 nm.

Narrow emitter mesa was formed by using the structure with emitter thickness of 30 nm. Emitter metal with 20-nm-thick Ti, 25-nm-thick Pt and 200-nm-thick Au was formed by liftoff technique using electron beam lithography. InP layer was etched by solution of $HCl:CH_3COOH$=1:4 at temperature of 3-5°C. Lateral undercut etching of 150 nm was restrained. The emitter structure of 100 nm width could be formed when emitter metal with width of 400 nm, as shown in Fig. 2.

Conventional InP DHBT with emitter along <010> direction was fabricated. Fabricated emitter widths were 100 nm, 300 nm, 500 nm, 1 μm and 2 μm. Electron beam lithography was used for patterning completely through the process. PMMA was used for liftoff as a positive type resist and RD2000N was used for protection of mesa at wet chemical etching as a negative type resist. Devices were buried by BCB for passivation and planarization. Contact windows were opened using reactive ion etching.

In the DC measurement, operation of transistor was confirmed when the emitter width were 500 nm, 1 μm and 2 μm. Figure 3 shows the common-emitter collector I-V characteristics of the device with 500-nm-wide emitter. Current gain of 50 was observed at V_C = 2 V and I_C = 0.25 mA. Figure 4 shows the dependence of f_T and f_{MAX} on emitter width. f_T was decreased with reduction of emitter size. f_{MAX} showed a peak point around the emitter width of 1 μm. These emitter width dependencies were typical characteristics of devices in which C_{BCT} was kept constant.

We could not observe the operation of the devices with 100-nm and 300-nm-wide emitter, because a thickness of BCB around the devices was dependent on mesa size, and the thickness of small area devices became too thin. Thus, opening of contact window adjusted for the narrow emitter will provide the operation.

References

[1] T. Arai, H. Tobita, Y. Harada, M. Suhara, Y. Miyamoto and K. Furuya: IPRM'99, TuA1-4, 1999, Davos, Switzerland.
[2] T. Arai, Y. Harada, S. Yamagami, Y. Miyamoto and K. Furuya: accepted to IPRM'00, TuB1., 2000, Williamsburg, Virginia, USA.
[3] T. Arai, H. Tobita, Y. Harada, M. Suhara, Y. Miyamoto and K. Furuya: MSS9, D21, 1999, Fukuoka, Japan.

Table 1. Epitaxial layers of HBTs.

Layer	Material	Thickness [nm]	Doping [cm^{-3}]
Contact	n-GaInAs	20	2×10^{19}
Emitter Emitter	n-InP n-InP	5, 5, 5, 5, 70 15,25,45,100,100	2×10^{19} 5×10^{17}
Base	p-GaInAs	50	2×10^{19}
Collector	i-GaInAs n-InP i-InP	60 5 200	2×10^{17}
Subcollector	n-GaInAs	600	1×10^{19}
Buffer	i-InP	100	

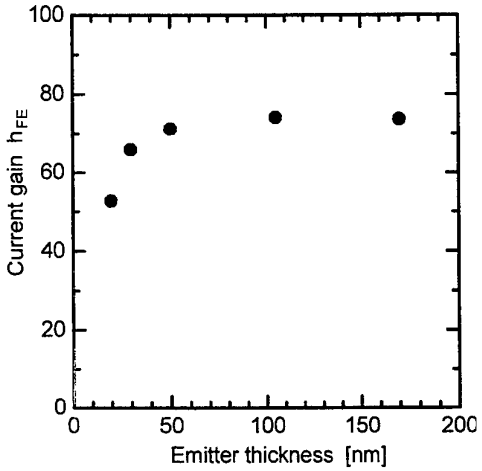

Figure 1. Dependence of current gain on emitter thickness of InP layer. Emitter width was 50×50 μm².

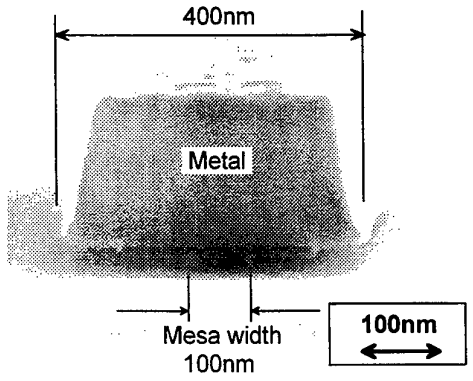

Figure 2. Test structure of emitter. Mesa width was 100 nm. Mesa was oriented toward <010> direction.

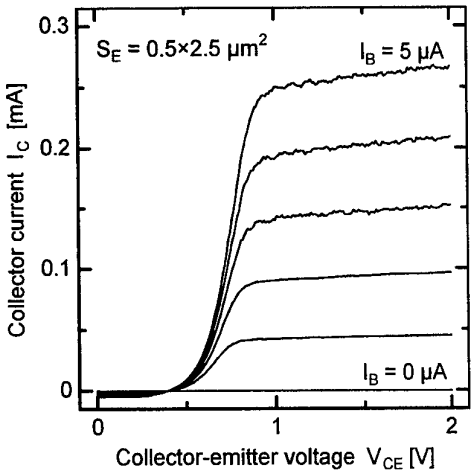

Figure 3. Common-emitter collector I-V characteristics. Emitter mesa area was 0.5×2.5 μm².

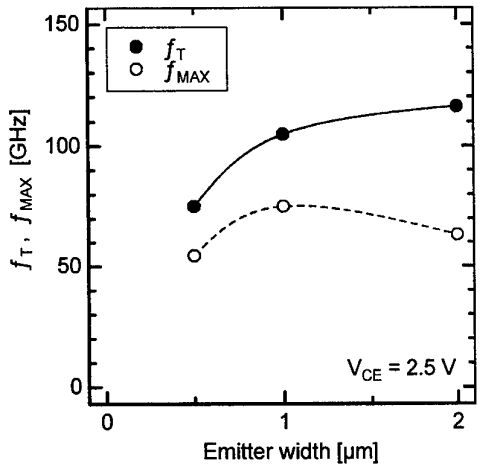

Figure 4. Dependence of f_T and f_{MAX} on emitter width.

Temperature compensation technique of InGaP/GaAs Power HBT with novel bias circuit using Schottky diodes

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Abstract

The temperature compensation technique of InGaP/GaAs power HBT with novel bias circuit using Schottky diodes is developed. The variation in the quiescent current to the temperature is less than 20% from –30℃ to 90℃ by this technique, while that is about 200% by the conventional bias circuit.

HBTs have been applied to power applications for personal digital cellular phone because of its superior high-frequency performances with single power supply. The bias circuit is usually used for the power HBT to supply the constant base bias voltage. Fig.1 shows the conventional bias circuit. As the temperature increases, the decrease of turn-on voltage of the emitter-base diodes has the same voltage shift as the HBTs. However the temperature dependence of quiescent current cannot be completely compensated by this bias circuit. Alternative approach to compensate the current increase is to use the large area emitter-base diodes, which ends up with increasing the current consumption in the bias circuit.

The newly developed bias circuit using Schottky diode is shown in Fig.2. The four staged Schottky diodes are used instead of the two staged emitter-base diodes, which make twice as large voltage shift to the temperature as the conventional ones. Fig.3 shows the temperature dependence of both diodes. The turn-on voltage of Schottky diode is 0.62V, while that of emitter-base diode is 1.20V, at $J=50A/cm^2$, 298K. On the other hand, their temperature coefficients are almost the same ($\Delta V/\Delta T= -1.37mV/K$). It is noted that the R1 resistance is also inserted in order to compensate the little difference of the turn-on voltages between four Schottky diodes and two emitter-base diodes.

The InGaP/GaAs power HBT amplifiers were fabricated, where WSi, Ti/Pt/Au and AuGeNi/Au metals are used for ohmic contact to emitter, base and collector, respectively. The emitter size is $60\mu m^2 \times 80$ cells. The Schottky contact on the n-collector layer can be formed at the same time with the base metalization as shown in Fig.4. It means no additional process is needed to fabricate Schottky diodes.

Fig.5 shows the resultant quiescent current of the newly developed bias circuit compared with the conventional one. The new bias circuit can achieve almost flat temperature characteristics from -30℃ to 90℃. It is noted that the current consumption of the newly developed bias circuit is reduced one third as little as that of conventional one.

Fig. 6 shows the temperature characteristics of RF performances of power HBT MMIC. The MMIC consists of two staged power HBT amplifiers with the newly developed bias circuits and the inter matching circuit. Gain, PAE and ACP are almost constant with the temperature.

In conclusion, the bias circuit using Schottky diodes has been developed in order to improve the temperature dependency of power HBT performances. This temperature compensation technique will contribute the expansion of power HBT market.

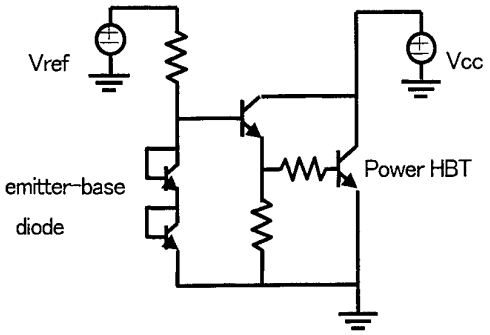

Fig.1 Conventional bias circuit using emitter-base diodes

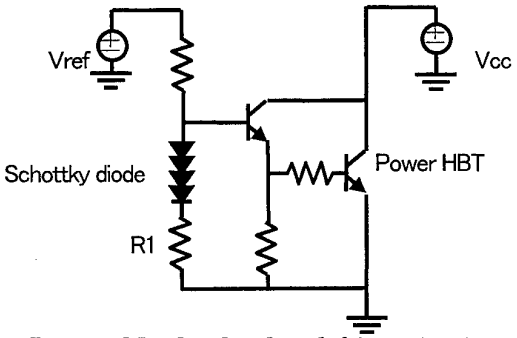

Fig.2 Newly developed bias circuit using Schottky diode

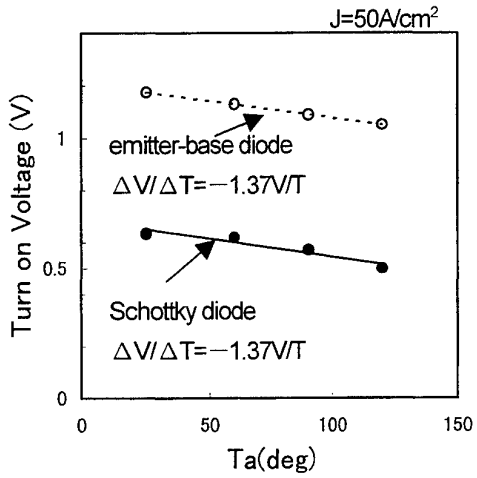

Fig.3 The temperature dependence of turn-on voltages at J=50A/cm²

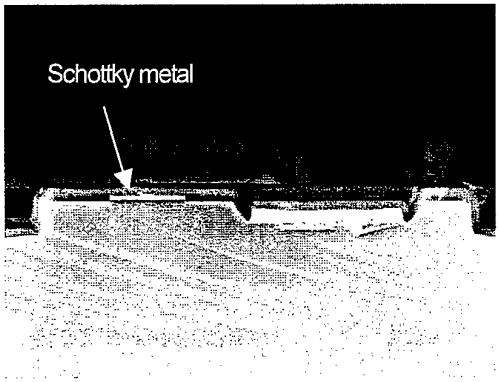

Fig.4 SEM photograph of the Schottky diode

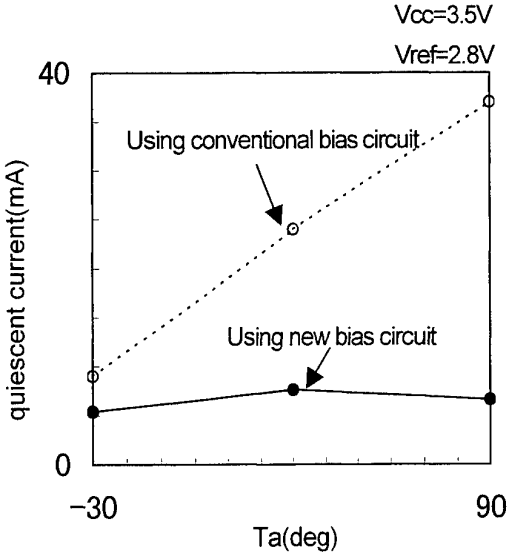

Fig.5 The temperature dependence of quiescent current.

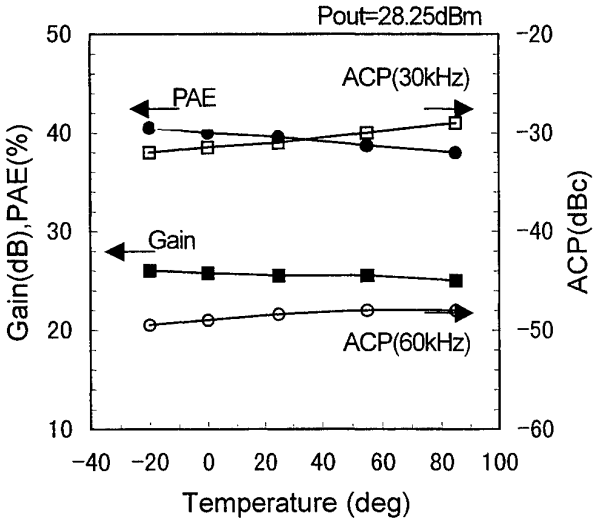

Fig.6 The temperature dependence of MMIC RF performance.

Nitride Passivated, X-Band AlGaAs/GaAs HBT's with TiW Emitter and Base Contacts

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Investigations into the reliability lifetime of heterojunction bipolar transistors operated at current densities above 50,000 A/cm^2 are essential for their commercial and military applications. As the operating power of these devices increases, good thermal management, diffusion free metal contacts, as well as a reduction in defects in epitaxial material are necessary to guarantee extended lifetimes of HBTs. Previously, we have studied the lifetime characteristics of Au emitter contact X-band devices shown in Figure 1. These devices were operated at 50,000 A/cm^2 emitter current density and their electrical parameters were monitored in-situ. The failure modes, which became prevalent during electrical stress, were degradation in the common emitter current gain and

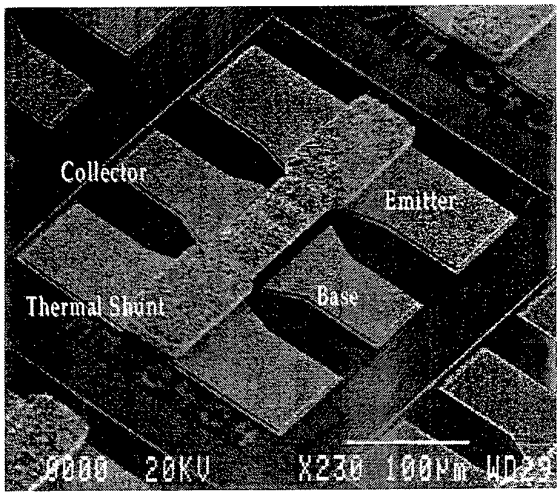

Figure 1. In-house fabricated, thermally shunted HBT.

increasing base current leakage as noted in the Gummel curves of the devices. The list of potential failure mechanisms causing base-emitter leakage and beta degradation include metal/GaAs reactions (temperature spiking of the contact metal), epi dislocations which create trapping sites, base dopant diffusion, recombination enhanced defect reactions, and dark line defects [1], [2], [3]. We found a strong correlation between material quality and lifetime. We determined this through analysis of two different epi lots of similar material structure from the same material vendor. These devices were passivated with polyimide and had a 15 micron thick thermal shunt contacting the emitter. One group of material (lot B) contained visible surface roughness in the emitter layers whereas the other group was smooth in appearance (lot A). Atomic force microscope (AFM) measurements as well as optical microscopy measurements using Nomarski filtering verified the roughness was below the top surface of the emitter InGaAs contact layer and appeared as dislocations. Transmission microscopy also revealed the presence of a high density of dislocations at the base-emitter junction on the rough material. Lot A had significantly fewer dislocations and a smoother base-emitter interface. The Au emitter devices operating at 50,000 A/cm^2 on the lower defect-density material (wafer lot A) have not failed after 5000 hours at 112°C junction temperature (with failure defined as a 20% reduction in the common emitter current gain). All of the Au emitter devices operating on the

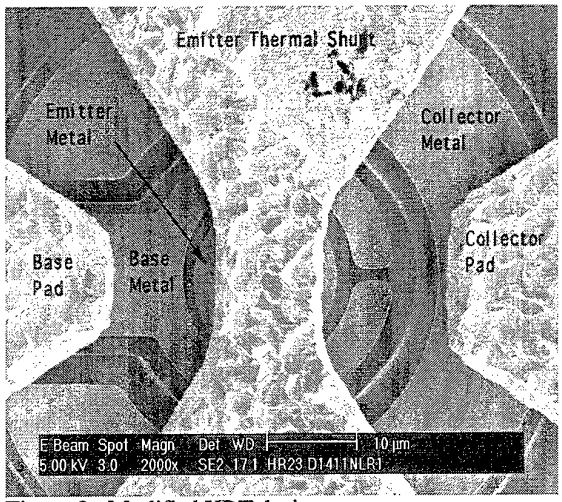

Figure 2. Modified HBT design.

higher defect density material (wafer lot B) failed between 100 and 400 hours, while operating under the same conditions as lot A.

As a result of these studies, a process test matrix was designed to compare the effects of refractory emitter and base contacts to standard Au emitter and TiPtAu base contacts, as well as comparing silicon nitride passivation versus no passivation over the base-emitter and base-collector junctions. The test matrix was performed on one epi lot from a single material vendor. Table 1 details the process flow and variations that were tested. The baseline comparison is the thermally shunted X-band device shown in Figure 1 and whose data (lot 1) is shown in the second

column of Table 1. This device had polyimide passivation and no nitride, and it's MTTF was 732 hours, where failure was defined as 20% degradation in the common emitter current gain. The last three columns represent devices fabricated using a modified mask set that allowed for easier characterization of the HBT through scanning electron microscopy and electroluminescence measurements, as shown in Figure 2. Lot 2 devices were fabricated using no dielectric over the junctions. The MTTF for these devices was significantly shorter at 325 hours. The fourth column (lot 3) represents devices with nitride passivation, gold emitter contacts and TiPtAu base contacts. These devices are presently under test and show very stable operation with only an 8% degradation in beta after 500 hours at 50,000 A/cm^2 current density. The final column (lot 4) represents TiW base and emitter contact devices with nitride passivation. These devices are also under test and show great promise. The refractory contacts and nitride passivated junctions should allow for the determination of true material failure versus contact degradation or surface leakage. The RF performance of the refractory contact devices is slightly degraded due to higher base contact resistance, however it is believed that these contacts can be optimized.

An additional failure signature noted in the stressed devices was a sharp decrease in the light emission at the base-emitter periphery. Both qualitative and quantitative measurements of this light output were obtained for both materials. These results agree with the computer simulations indicating that the current density and recombination rate are peaked at the emitter-base periphery. The nitride passivated devices show a significantly narrower electroluminescence peak with a falloff of 23 - 30 meV/decade as compared to the devices without nitride whose falloff is 110 meV/decade. This result is significant, and degraded devices are being analyzed to determine if this peak spreads out during high current density stress. If so, that would indicate that the AlGaAs/GaAs heterojunction may be degrading.

In conclusion, the beta degradation and base leakage failure modes are strongly related to the poor epi material and insufficient passivation of base-emitter surface states. The refractory based contact devices with nitride passivation show strong promise as a process to characterize true HBT material quality. Long term stress studies of these devices at high current density operation are underway to determine the activation energy for material degradation. This degradation will be characterized using electroluminesence as well as focused ion beam cross-sections and TEM analysis of the base-emitter junction.

Table 1. Process matrix utilizing wafers from a single epitaxial run.

PROCESS	LOT 1 BASELINE	LOT2	LOT 3	LOT 4
Emitter Metal	Au Plated	Au Plated	Au Plated	TiW Sputtered
Emitter Etch Process	Citric Acid/H_2O_2	Citric Acid/H_2O_2	Citric Acid/H_2O_2	Citric Acid/H_2O_2
Base Mesa Etch Process	Citric Acid/H_2O_2	Citric Acid/H_2O_2	Citric Acid/H_2O_2	Citric Acid/H_2O_2
Isolation Etch Process	Citric Acid/H_2O_2	Citric Acid/H_2O_2	Citric Acid/H_2O_2	Citric Acid/H_2O_2
Collector Metal	NiGeAuNiAu	NiGeAuNiAu	NiGeAuNiAu	NiGeAuNiAu
Base Metal	TiPtAu	TiPtAu	TiPtAu	TiW
Nitride Passivation	None	None	Plasma CVD	Plasma CVD
Nitride Etch Process	N/A	N/A	N/A	CF_4O_2 RIE
Base/Emitter Metal	N/A	N/A	N/A	Sputtered
B/E Metal Etch Process	N/A	N/A	N/A	CF_4O_2 RIE
Thermal Bridge Support	Polyimide	None (Air Bridge)	Polyimide	Polyimide
Bridge Thickness	12 µm Au	7 µm Au	9.7 µm Au	9.1 µm Au
Emitter Contact Resistance (ohm-mm)	0.048	0.059	0.074	0.133
Base Contact Resistance (ohm-mm)	0.123	0.348	0.186	0.99
Collector Contact Resistance (ohm-mm)	0.071	0.027	0.035	0.032
Emitter Sheet Resistance (ohm/sq)	25.9	21.5	23.9	26
Base Sheet Resistance (ohm/sq)	286	340	275	399
Collector Sheet Resistance (ohm/sq)	11	13.4	14.7	14.9
Thermal Resistance (°C/W)	270	344	320	420
F_T (GHz)	35.1	32.4	33.4	31.5
F_{MAX} (GHz)	36.0	31.5	29.9	23.5
EL Base-Emitter Peak (eV)	Not Measured	1.35	1.35	1.36
Spectral Falloff (mev/dacade)	Not Measured	110	30	23
MTTF @ 50KA/cm^2 (hrs)	732	325	>350 (Testing)	>350 (Testing)

The authors greatly acknowledge support provided by AFOSR.

[1] Liu, W. (1998). *Handbook of III-V Heterojunction Bipolar Junction Transistors.* New York: John Wiley & Sons, Inc.

[2] Kayali, S., Ponchak, G., and Shaw, R. (1996). *GaAs MMIC Reliability Assurance Guidelines for Space Applications.*, p. 93.

[3] Sugahara, H., Nagano, J., Nittono, T., and Ogawa, K. (1993). *Tech. Dig. GaAs IC Symp., p. 115.*

Low V_{be} GaInAsN Base Heterojunction Bipolar Transistors

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The turn-on voltage of an HBT, typically defined as the base-emitter voltage (V_{be}) required to achieve a certain fixed collector current (I_c), is an important figure of merit describing the forward characteristics of the base/emitter junction. Ideally, the turn-on voltage of an HBT is governed by the material properties of the base layer. However, a spike in the conduction band at the emitter-base interface can block electron transport, thus limiting the collector current and effectively raising the turn-on voltage. With proper materials engineering, the effective height of the conduction band spike at a heterojunction can be significantly reduced. State-of-the-art InGaP/GaAs and AlGaAs/GaAs HBTs have collector currents which are indistinguishable from GaAs BJTs of similar base sheet resistance (R_{sb}). Further reductions in the turn-on voltage require a lower energy-gap base layer.

In this work, we report on the use of an exciting new material system, GaInAsN, to break the lower barrier on the turn-on voltage of GaAs-based HBTs. Numerous laboratories have demonstrated that the energy-gap of GaInAs drops substantially when small amounts of N are incorporated into this alloy [1]. Moreover, because N pushes the lattice constant in the opposite direction from In, GaInAsN alloys can be grown lattice-matched to GaAs, and thus eliminate the problems associated with excess strain. We describe here InGaP/GaInAsN HBTs which exhibit a 10 mV reduction in turn-on V_{be} (corresponding to a 2x increase in J_c), while still maintaining high p-type doping levels (> 3E19 cm^{-3}) and peak dc current gain (> 45 @ R_{sb} = 272 Ω/□). The reduction in turn-on V_{be} enabled by GaInAsN base layers should allow for better management of the voltage budget on both wired and wireless GaAs-based RF circuits, which are constrained either by standard fixed voltage supplies or by battery output. Lowering the turn-on V_{be} also alters the relative magnitude of the various base current components, allowing for more stable dc current gain as a function of both J_c and temperature, and may also increase long term device reliability [2,3]. Finally, strain-free, graded energy-gap GaInAsN base structures can be reasonably expected to enhance RF performance.

Figure 1 plots the turn-on voltage (@ J_c = 1.78 A/cm^2) as a function of R_{sb} for a number of InGaP/GaAs HBTs, GaAs/GaAs BJTs, and InGaP/GaInAsN HBTs. All samples have MOCVD-grown, C-doped base layers varying between 1.5-6.5E19 cm^{-3} in doping and 500-1500 Å in thickness. Large area devices (L = 75 μm x 75 μm) were fabricated using a simple wet-etching process and tested in the common base configuration [2]. The turn-on V_{be} of both the InGaP/GaAs HBTs and the GaAs emitter/GaAs base BJTs, which clearly do not have any conduction band spike, qualitatively exhibit the same ideal logarithmic dependence on R_{sb}. The turn-on V_{be} of the InGaP/GaInAsN HBTs also follows a logarithmic dependence on R_{sb}, but is shifted downward by 11.5 mV. The dc current gain measured at 1kA/cm^2 is near 50, which is the highest ever reported for this type of base layer. As exemplified by the Gummel plots overlaid in Figure 2, the collector currents of the InGaP/GaAs HBTs and GaAs/GaAs BJTs with similar R_{sb} are indistinguishable for over five decades of current until differences in effective series resistance impact the current-voltage characteristics. On the other hand, the collector current of a comparable InGaP/GaInAsN HBT is 2x higher than the standard GaAs base structures over a wide bias range. The energy-gap reduction in the GaInAsN base, assumed to be responsible for the observed reduction in V_{be}, has been confirmed by low temperature (77 K) photoluminescence (Figure 3). DCXRD measurements indicate the lattice mismatch of the base layer is minimal (< 150 arcsec).

These results clearly indicate the potential of GaInAsN materials for lowering the turn-on voltage in GaAs-based HBTs. This work is supported by WPAFB via STTR funding (contract # F33615-99-C-1510).

[1] K. Nakahara *et al.*, Electon. Lett. **32**, 1585 (1996).
[2] R. E. Welser *et al.*, to be published in IEEE Elec. Dev. Lett. (May 2000).
[3] R. E. Welser *et al.*, to be published in Proc. GaAs MANTECH, Washington D.C. (May 2000).

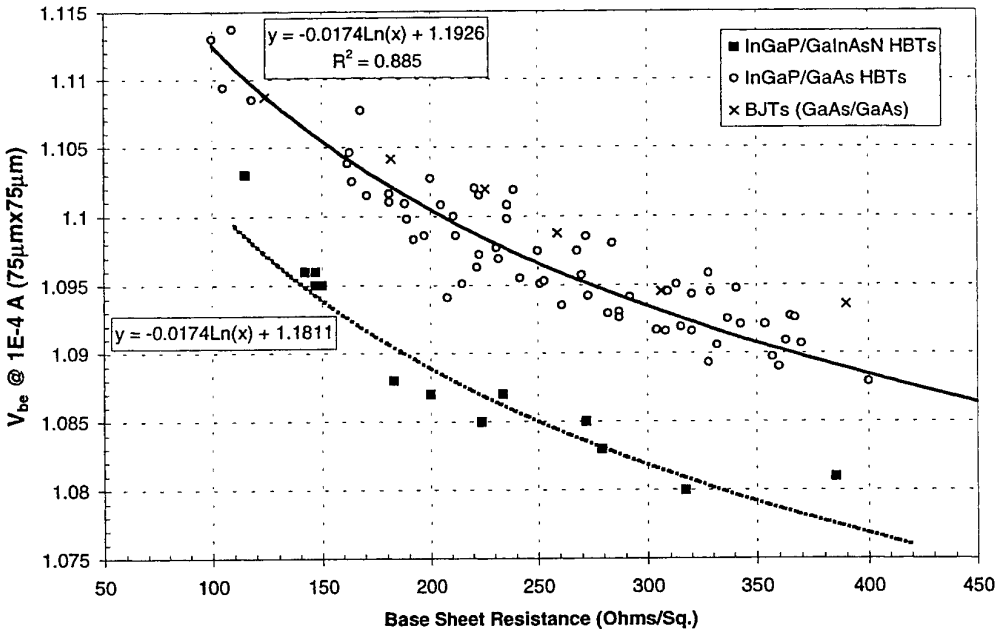

Figure 1: Turn-on V_{be} (@ $J_c = 1.78A/cm^2$) as a function of R_{sb} for standard InGaP/GaAs HBTs, GaAs/GaAs BJTs, and InGaP/GaInAsN HBTs. The solid line represents a logarithmic fit to the InGaP/GaAs HBT data, while the dashed line is a 11.5 mV reduction to the fit, used as a guide for the eye for the InGaP/GaInAsN data.

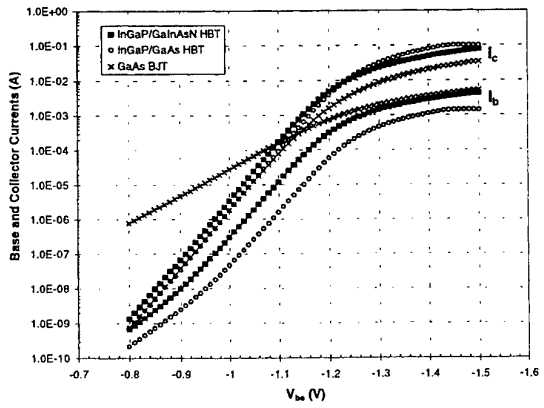

Figure 2: Gummel plots from a standard InGaP/GaAs HBT, GaAs/GaAs BJT, and InGaP/GaInAsN HBT (L = 75 µm x 75 µm) with comparable R_{sb} (~ 250 Ω/□).

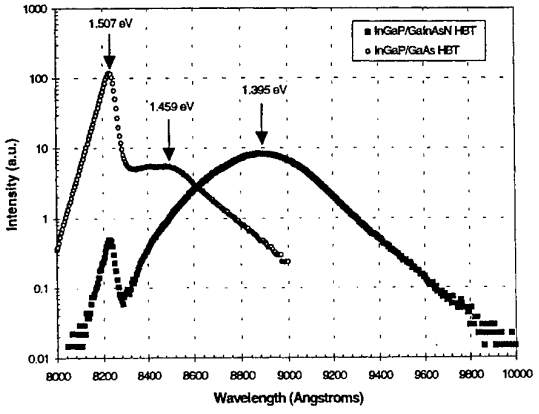

Figure 3: Liquid N_2 PL spectrums from a standard InGaP/GaAs HBT and a InGaP/GaInAsN HBT, both with a nominal base thickness of 1500 Å. PL spectrums were taken after etching down to the InGaP emitter. The positions of the n-type GaAs collector (1.507 eV) and the p-type base layer peaks are marked (1.459 eV and 1.395 eV).

HBT Base Layer Characterization Using Spectrally Resolved Electro-Luminescence

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Photoelectric techniques, such as photoluminescence (PL) are commonly used in the characterization and analysis of heterostructure material[1] for use in heterostructure bipolar transistors (HBTs). These techniques provide vital information on the energy band profiles of heterostructures. These routinely used techniques are not applicable to the evaluation of fully fabricated HBTs since the transistors are very small and the surface of the transistor is covered with metal. Yet, it is important to obtain accurate energy information on fully fabricated HBTs. The energy configuration depends on applied bias voltages, high temperature processing may modify the band profiles, mechanical stress causes piezoelectric effects in these structures, and the band configuration may be altered due to electrical stress when the device is operated at high current density. In this paper, we describe spectrally resolved electroluminescence studies to gain understanding of the energy bands in fully fabricated HBTs. Electroluminescence has been used in the past to study semiconductor junctions.[2]

The measurements are performed on wafer on a probe station at room temperature. The devices studied have a circular window in the emitter metal (Figure 1) to allow luminescent light to escape from the surface. One end of an optical fiber is located a few millimeters above the transistor while the other end is mounted at the entrance slit of an Acton Research 150 monochromator. A silicon photodetector is placed at the exit slit. The current, generated in the detector is amplified, using a low noise current preamplifier and measured, using a lock-in amplifier. The base and collector bias currents and voltages are supplied with a HP4142 parameter analyzer. Pulsed currents and voltages are used to allow detection by the lock-in technique.

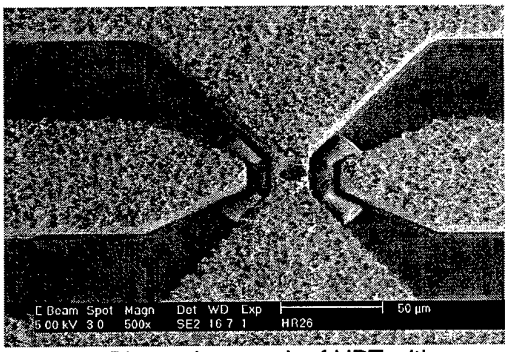

Figure 1 Photomicrograph of HBT with circular window in emitter metal

In this paper, results from GaAs based HBTs are presented. The materials structure was grown by MOCVD and was identical for all wafers. A graded AlGaAs wide bandgap emitter is used. The GaAs base is 80 nm thick and contains a carbon doping concentration of $4x10^{19}$ cm^{-3}. The collector consists of a 1250 nm, $1x10^{16}$ cm^{-3} doped GaAs layer on top of a heavily doped sub-collector. A thermal shunt provides for uniform heating of the structure. Various ohmic metal and passivation layers are used in the HBT fabrication processes.

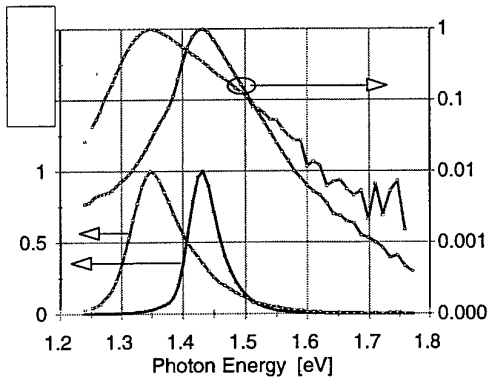

Figure 2 Electroluminesence spectra of base (low energy peak) and collector in logarithmic and linear representation

Figure 2 shows the spectral characteristics of the luminescence light, generated in the base and the collector layers of an HBT. Electroluminescence results from the injection of minority carriers into a semiconductor. The base

emission is obtained by applying a positive collector/base voltage and pulsing the base current to turn the transistor on. The collector/base voltage eliminates hole injection into the base. The collector spectrum results from forward biasing the collector/base junction, causing hole injection into the collector. The graph indicates that the spectral characteristics of the base and collector layers are different. As expected, the collector spectrum is narrow (FWHM: 50 meV) and has steep fall-off in the logarithmic representation due to the Boltzmann distribution of electrons (60 meV/decade), indicating high quality, low doped GaAs material. The peak occurs at the GaAs band energy (1.43 eV). The base spectrum shows the peak at a significantly lower energy (1.35 eV), the spectrum is much wider (FWHM: 100 meV) and the fall-off in logarithmic format is less steep (150 meV/decade). These findings are consistent with the high carbon doping concentration in the base layer, leading to significant stress and bandgap narrowing. The base spectra depend critically on device fabrication processing while the collector spectra are independent of it. No other spectral lines were observed. Specifically, we were not able to observe an indirect transition from emitter to base, which was identified by Lu[1], using PL.

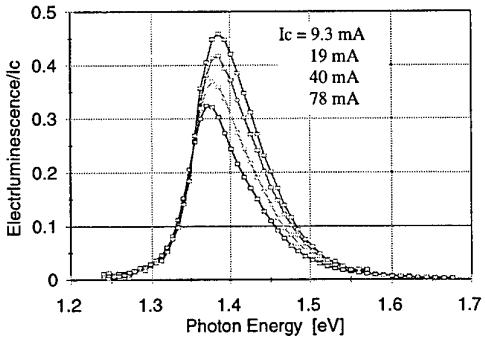

Figure 3 Base electroluminescence spectra normalized to the collector current as a function of collector current

Figure 4 shows the base spectra of an HBT before and after electrical stress. The device was stressed at 50 kA/cm^2 for many hours. Due to this stress, the device characteristics degraded: The base current increased and the gain decreased. These data suggest that the base layer of this HBT degraded, causing the change in device characteristics.

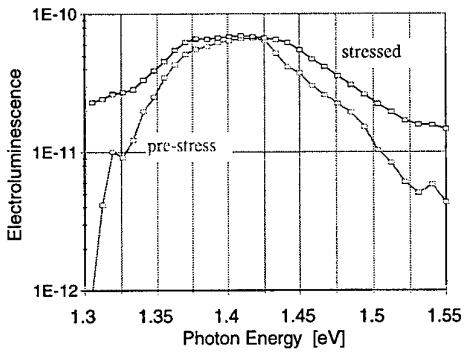

Figure 4 Base electroluminescence spectra of the pre-stress and stressed transistor

The examples shown in this abstract indicate that the electroluminescence spectra of both base and collector can be accurately measured and that these data provide valuable information on the configuration of the structures. In this paper we will correlate the spectral characteristics with device performance and transistor processing.

The authors gratefully acknowledge support by AFOSR.

[1] Lu, Z.H., Majerfeld, A., Yang, L.W. IEEE Journal of Selected Topics of Quantum Electronics 1, 1030 - 1036 (1995).

[2] Tian, S.X., Haneman, D., Nozaki, S., and Takahashi, K.. Appl. Phys. Lett. 66, 1246 – 1248, (1995)

HBT Collector Characterization by the Spectral Photocurrent Technique

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Heterostructure bipolar transistors (HBTs) are being developed for applications where high performance is of critical importance. Optimization of the collector is required to obtain the desired device characteristics. New and improved techniques are needed to characterize these structures. We have demonstrated[1,2] that the spectral photocurrent technique is an excellent tool to profile heterojunctions. The purpose of this paper is to compare photocurrent results of three types of HBT collectors, containing GaAs, InGaP, and AlGaAs layers.

The transistors studied had a window etched in the emitter metal to allow illumination of the active transistor area. Since the measurements are performed under bias conditions where device currents are small, the heavily doped emitter contact layer provides sufficient current access in the window area. The measurements are performed on-wafer on a probe station. Chopped, monochromatic light is focused through a microscope into the emitter window. Figure 1 explains the various contributions to the photocurrents. The electric field in the depleted layer separates the photogenerated carriers. The holes and electrons are collected at the base and collector, respectively. Carriers, generated in the un-depleted regions have less than unity probability to contribute to the photocurrent. Electron and hole barriers affect these currents. The dependence of the photocurrents on photon energy and applied bias voltage gives insight into the energy configuration of these junctions.

In this study, three types of collector/base junctions were investigated. Table 1 describes their collector composition. All collectors contain a heavily n-doped sub-collector. The InGaP and AlGaAs structures are compound collectors, consisting of the wide bandgap material on top of a low doped GaAs layer. Grading layers are employed in the AlGaAs collector. Figure 2 presents the spectral characteristic of the collector/base junction of the HBT, containing the GaAs collector. The figure shows a sharp decay of the photoyield at the bandgap of GaAs with a drop-off of 30 meV/decade. The curve replicates the absorption behavior of high quality GaAs with only small doping concentration. This finding is consistent with photogeneration in the lightly doped collector layer. The photogeneration in the collector region is larger than in the

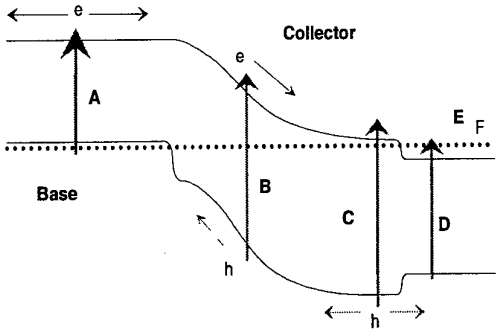

Figure 1. Energy diagram of base/collector junction, indicating optical excitation in different parts of the structure.

Table 1. Collector Structures

Description	Doping Concentration [cm^{-3}]	Thickness [nm]
GaAs Collector		
n GaAs	$7x10^{15}$	700
n GaAs	$5x10^{18}$	1000
InGaP Collector		
n GaAs	$3x10^{16}$	30
n GaAs	$2x10^{18}$	5
n InGaP (0.5)	$3x10^{16}$	265
n GaAs	$3x10^{16}$	400
n GaAs	$5x10^{18}$	1000
AlGaAs Collector		
n AlGaAs Grading	$3x10^{16}$	100
n AlGaAs (0.25)	$3x10^{16}$	120
n AlGaAs Grading	$3x10^{16}$	80
n GaAs	$3x10^{16}$	400
n GaAs	$5x10^{18}$	1000

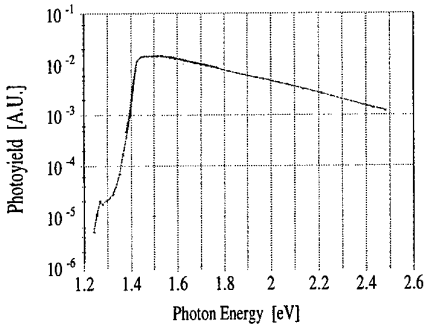

Figure 2. Photoyield vs photon energy of the GaAs collector at a junction voltage of 0 V

base since their volumes are vastly different. Figure 3 provides the dependence of the collector/base photocurrent, measured at hν = 1.61 eV on the collector to base voltage. One observes that the photocurrent remains constant at positive voltages (i.e. reverse voltage). Only when the junction is turned on hard at approximately –0.75 V is a decrease in photocurrent observed. From capacitance voltage measurements we know that the depletion region in the collector changes over this voltage range. The observed saturation in photocurrent indicates that both the depleted and un-depleted areas of the collector contribute equally to the photocurrent. The hole barrier at the n/n^+ junction in the collector plays an important role in directing the photo generated holes toward the base. Capacitance voltage measurements agree with the material parameters and indicate depletion widths of 250 and 550 nm at –0.75 and +1 V respectively.

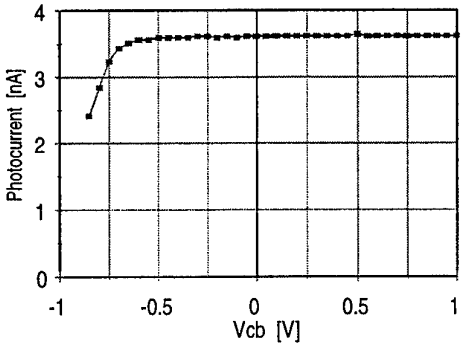

Figure 3. Dependence of the photocurrent of the GaAs collector on junction voltage

Figure 4 presents the spectral characteristics of the AlGaAs collector/base junction for three junction voltages: Vcb = +1, 0, and –0.6 V. The curves are plotted both in logarithmic and linear format. The +1 and 0 V curves have GaAs like character with very steep fall-off at the band edge (30 meV/decade). This indicates that the photocarriers are generated in the very pure, low doped GaAs collector layer. Photogenerated holes in this layer travel through the AlGaAs to the base. In contrtast, the InGaP collector layer formed an effective hole barrier. At Vcb = -0.6 V, the fall-off at the GaAs band edge is 115 meV/decade, a much larger value than observed a 0 and +1 V. These findings suggest that at Vcb = -0.6 V, the AlGaAs layer forms an effective hole barrier and that the photocurrentcurrent stems from photo-generation in the base. In Figure 5, the dependence of the photocurrent on the collector base voltage at two photon energies, 1.5 and 1.8 eV is shown. The curves suggest that at Vcb > 0.5 V, the AlGaAs layer is transparent to the holes, photogenerated in the GaAs collector.

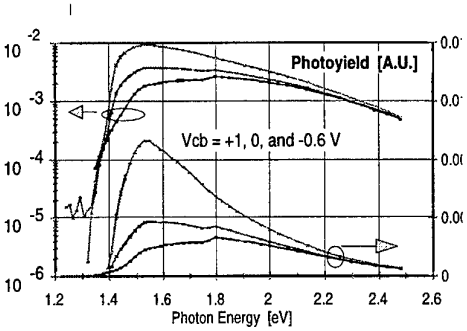

Figure 4. Spectral photoyield of AlGaAs collector for three junction voltages

In this paper, we will contrast the measurement results, obtained on the three collector structures, studied. The spectral photocurrent technique provides an excellent tool to obtain energy profiles of heterostructuress. Also, we are able to evaluate the effects of hole currents. This is important since holes are generated by impact ionization during device operation. We will compare CV and photoconduction profiling techniques.

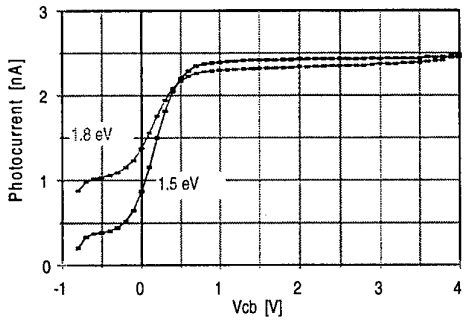

Figure 5. Dependence of the photo-currents of the AlGaAs collector on junction voltage

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[1] Fritz Schuermeyer et al, "Characterization of Heterostructure Bipolar Transistors by the Spectral Photocurrent Technique," 1999 International Semiconductor Device Research Symposium (ISDRS) Proceedings pp. 523 – 526, Charlottesville, VA, 1999

[2] Fritz Schuermeyer, Peter J. Zampardi and Peter M. Asbeck, "Photoemission studies on heterostructure bipolar transistors," Solid State Electronics, 43, pp. 1555-1560, 1999

Tunneling at the Emitter Periphery in Silicon Germanium HBTs

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In Silicon-Germanium HBTs typical Gummel plots show a region in the base current at low bias that is non-ideal. This component is accounted for in the SPICE Gummel –Poon model by a second term which has an ideality whose default value is 2. In reality the ideality factor in this region is >2 which indicates that its origin is not simply due to recombination [1]. This is confirmed by the fact that it appears to be weakly temperature dependent [1]. This suggests that a tunneling process is involved. There are at least 2 regions where tunneling may occur between the emitter and the base: in the space charge region defined by the emitter area and the perimeter of the emitter between it and the p-doped extrinsic base. In our devices (Fig.1), around the emitter the Si is *p* doped, in particular adjacent to the emitter window, by the boron out diffusion during processing, whereas under the emitter window the *p*-doping is compensated by the n^+ diffusion from the polysilicon emitter. Thus laterally, away from the emitter window, there is a narrow n+-p+ region, all around the emitter periphery - this high-field region is a consequence of the fabrication procedure, as in other reports, and is typical for Si bipolar devices [2]. Hence there is a significant built-in field around the edge of the emitter and a corresponding narrow depletion region.

Because the region involved in the tunneling is crucially dependent on the lateral diffusion and compensation of dopants, it is extremely sensitive to the processing conditions and also the interface between SiO_2 emitter window and the base. Although variations with emitter periphery and area occur (Fig. 2) the observations are not conclusive unless good statistics are obtained [2]. We have also seen variations in the low bias base current in pinched base devices where, in a device with 2 emitters, you can contact either a base contact around the emitters or between them (Fig.3). Although this is interesting from a device physics point of view it is really a part of a broader issue – that of device reliability. If we reverse bias stress the base-emitter of a device the emitter-base diode characteristics change and so too the low-bias base current (Figs. 5,6). This has been well-studied in Si BJTs [3,4]. In this paper we will show some of our stress and device dependent studies of peripheral tunneling in the low base current region of our SiGe HBTs.

[1] S. P. McAlister, S. Kovacic , A. Renaud and Z. F. Zhou, *J. Vac. Sci. Tech A*, **18**, 770 (2000)
[2] G.P. Li, E. Hackbarth and T.C. Chen, *IEEE Trans. Electron. Devices*, **35**, 89 (1988).
[3] D.R. Collins, *IEEE Trans. Electron. Devices*, **16**, 403 (1969).
[4] A. Neugroschel, C.T. Sah and M.S. Carroll, *IEEE Trans. Electron. Devices*, **43**, 1286 (1993).

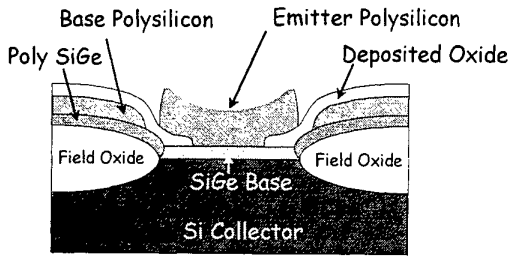

Fig. 1. Schematic diagram of the SiGe HBTs devices. SiGe profile is triangular.

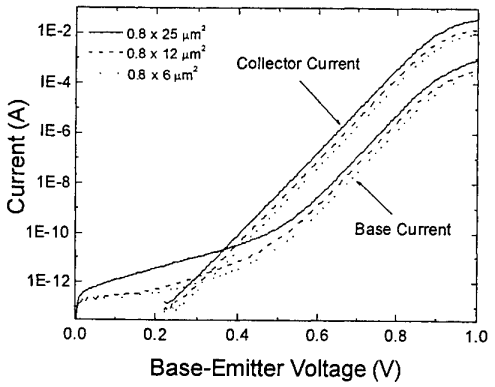

Fig. 2. Gummel plots for a series of devices which do show the low voltage base current dependent on emitter lengths.

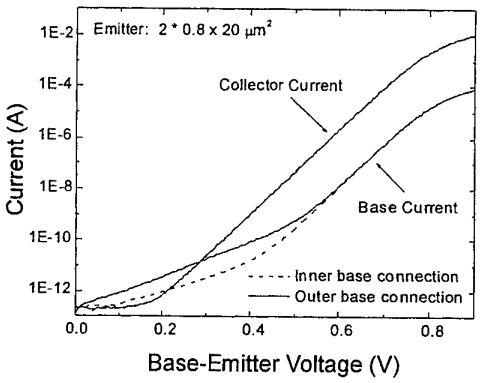

Fig. 3. Gummel plot for a pinched base device measured by contacting either the inner or outer base contacts.

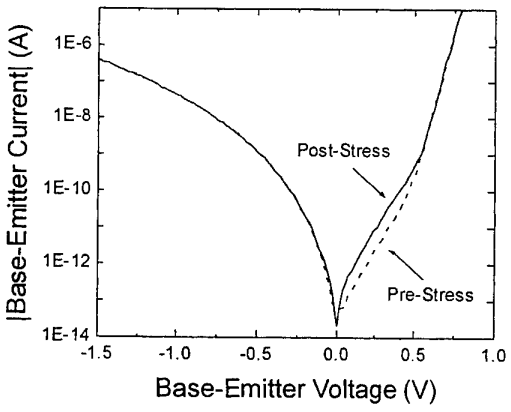

Fig. 4. The absolute value of the emitter-base diode current before and after the reverse-bias stress. The collector and base were connected together and –2.5V was applied to the emitter for 3000 secs.

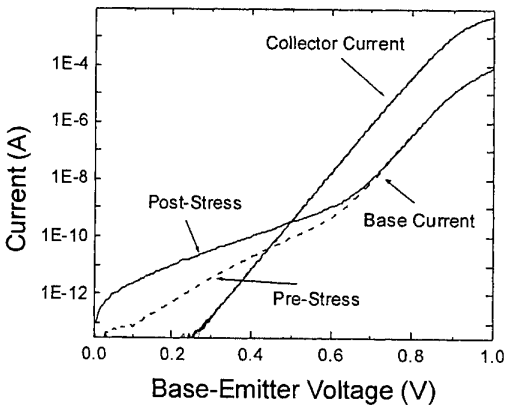

Fig. 5. Gummel plot for the device used for Fig. 4, before and after the application of stress. The emitter area was 0.8 x 3 μm^2.

High-Efficiency Reliable SiGe Microwave Power Heterojunction Bipolar Transistor

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Recent developments in SiGe HBT technology and device optimization lead to a maximum transit frequency and maximum frequency of oscillation of 130 GHz[1] and 160 GHz[2], respectively. A. Schuppen et al.[3] reported the power SiGe HBT for wireless applications, the SiGe HBT consists of 60 emitter stripes with an emitter-ballasting resistor of 6 Ω for each. P. A. Potyraj et al. [4] fabricated S-band SiGe power HBT with TiW emitter ballasting resistor for each emitter stripe, and indicated no reliability problem with the SiGe HBT by comparing the current gain and junction leakage before and after variable temperature test and accelerated life test.

It is of great importance to improve the power-added efficiency (PAE) of the power amplifier. One way to improve the PAE of the SiGe power HBT is to remove the emitter-ballasting resistor due to its internal mechanism to equalize the current distribution. In order to decide the reliability of the emitter-ballasting-resistor-free microwave power SiGe HBT, forward bias burn-in test was applied to the SiGe HBT, and RF measurement indicated no reliability problem with the emitter-ballasting-resistor-free microwave power SiGe HBT.

Figure 1 is the schematic cross sectional view of the emitter-ballasting-resistor-free SiGe HBT. The emitter is interdigitated and composed of 60 stripes with area of 6x40 μm^2 for each stripe. The die was packaged in metal-ceramic package. The detailed process was reported in Ref. 5. The output characteristics of the power SiGe HBT is shown in Fig. 2. No current crush is observed on the I-V output characteristics due to the high thermal conductivities of both the silicon substrate and the package. The current gain is about 69 and does not change when the collector current increases from 100 mA to 415 mA at collector-emitter voltage Vce of 2.5 V, as shown in Fig. 3.

The peak junction temperature was measured by infrared microscope. Figure 4 shows the peak junction temperature dependence of the HBT on the applied DC power. It is clear that the peak thermal resistance of the SiGe HBT is 22°C/W.

Figure 5 shows the continuos wave output power and PAE vs. the input power for common emitter SiGe HBT power amplifier. When the input power is 0.9 W, the output power reaches 5.4 W, the PAE reaches 64%, and power gain is 8 dB. Hence, the emitter current density of the emitter-ballasting-resistor-free SiGe HBT with emitter width of 6 μm is 0.975 A/cm at frequency of 900 MHz and bias voltage V_{ce} of 14 V, and the SiGe HBT has higher PAE than Si power BJT.

After 256 hrs of forward-bias burn-in tests (Vce = 10 V, Ie = 0.48 A) (Vce = 10 V , Ie = 0.61 A) which stress the peak junction at 170°C and 200°C respectively, the characteristics of the SiGe HBT does not change. We applied burn-in test with Vce of 10 V and Ie of 0.7 A on the SiGe HBT, which stresses the junction at 220°C. After 100 hrs of burn-in test, the leakage currents of the emitter junction and collector junction increase about 50 times that before burn-in test, and the current gain decreases rapidly, especially at small collector current. The output power and PAE decrease after the burn-in test, as shown in Fig. 5.

Therefore, the emitter-ballasting-resistor-free microwave power SiGe HBT has high PAE, and has no reliability problem when the junction temperature is not higher than 200°C, which is the same as Si power BJT.

References

1, K. Oda, E. Ohue, M. Tanabe, et al. IEDM Tech. Dig., pp.791-794, 1997.
2, A. Schuppen, U. Erben, A. Gruhle, et al. IEDM Tech. Dig., pp. 743-746, 1995.
3, A. Schuppen, S. Gerlach, H. Dietrich, et al. IEEE Microwave and Guided Wave Letters. vol. 6 (9), pp. 341-343, 1996.
4, P. A. Potyraj, K. J. Petrosky, K. D. Hobart, et al. IEEE Trans. on Microwave Theory and Techniques, vol. 44, no. 12, pp. 2392-2397, 1996.
5, Jinshu Zhang, Hongyong Jia, Pei-Hsin Tsien et al. IEEE EDL No.7, 1999.

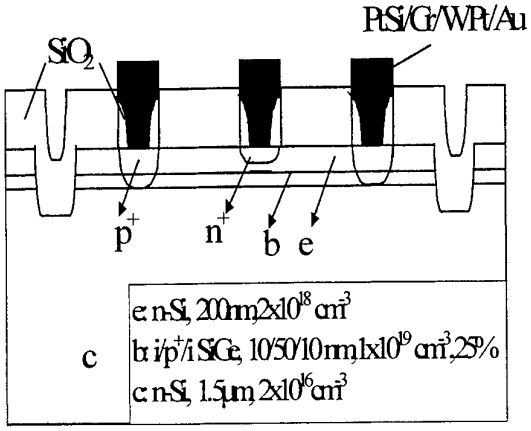

Fig. 1 Schematic cross sectional view of the SiGe HBT.

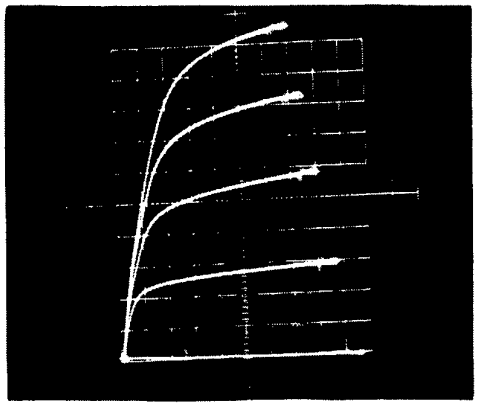

Fig. 2 Output characteristics of the power SiGe HBT. Where horizontal axis stands for 0.5V/div, vertical stands for 50 mA/div, and base current step is 2 mA.

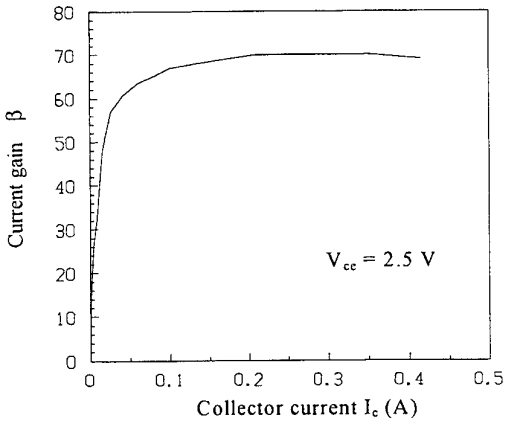

Fig. 3 Current gain dependence on the collector current of the SiGe HBT.

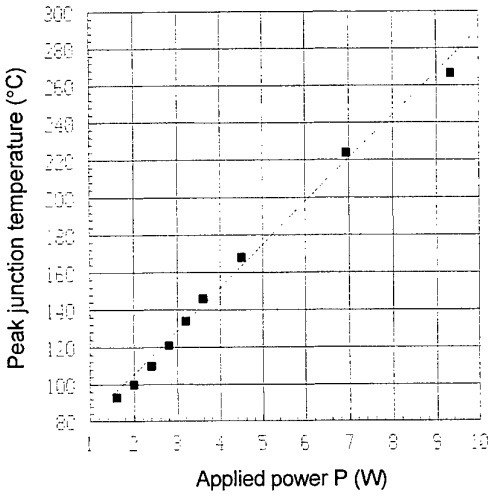

Fig. 4 Peak junction temperature dependence on the applied DC power.

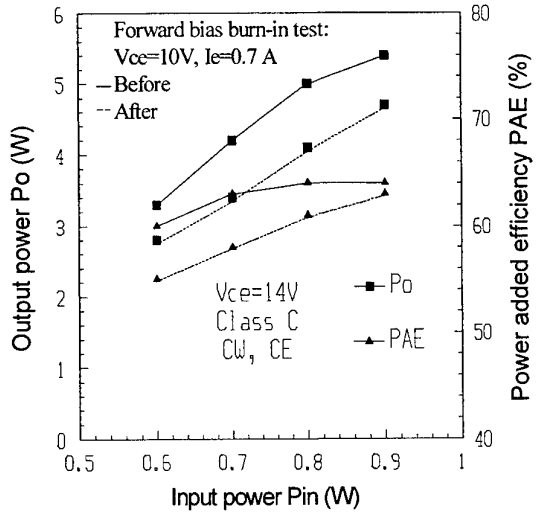

Fig. 5 Continuos wave output power and power added efficiency vs. the input power for common emitter SiGe HBT power amplifier, working in Class C operation at the frequency of 900 MHz and bias voltage V_{ce} of 14 V, before and after forward bias burn-in test.

A 5.8 GHz Si/SiGe VCO with Amplitude Control for Wireless LAN Applications

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ABSTRACT: We present a 5.8 GHz VCO for the 5 GHz HIPERLAN band. The VCO uses a center-tapped inductor and a substrate shield to improve phase noise. Sensitivity to supply voltage and temperature is reduced by an amplitude control block. The design is based on a distributed inductor model which allows optimization without antecedent inductor measurements. The circuit is fabricated in a 0.8 μm 45 GHz f_T SiGe-HBT technology and operates with a supply of -2.0 V to -3.3 V.

I. Introduction

For wireless LAN data rates above 10 Mb/s are necessary to interface with Ethernet or ATM and to meet the user demand for high bandwidth. In the 2 GHz band such data rates are difficult to achieve for a large number of channels, therefore the 5 GHz band has been chosen for the HIPERLAN standard. We use a SiGe-HBT technology because it allows to design low-power, low noise RF circuits [1, 2].

II. Design Considerations

It is our goal to develop a 2.7 V 5.8 GHz WLAN transceiver-chip. In a first step we test building blocks to understand the influence of layout on the chip function. Additionally we aim to dispense with time consuming and costly antecedent inductor tests, thus much effort is also spent on modeling of integrated inductors.

Testing building blocks causes a trade-off between design "for system" and "for test", because the testing equipment has some impact on the design. For measurement of an oscillator an output buffer is necessary to disable negative effects of reflections or asymmetrical loads at the differential output on center frequency and phase noise. Due to the large resonator voltage a buffer will normally operate as a limiter, therefore the actual resonator voltage could not be measured directly. To overcome this problem we scale down the resonator voltage so that the buffer operates in the linear region and thus provides more information about the interior.

III. Oscillator Schematic

We recommend a fully differential oscillator to improve phase noise and to reduce sensitivity to common-mode signals. The use of a center tapped inductor (CTI) is advantageous for this type of oscillator because the grounded center tap is on a virtual ground and does not reduce the quality factor. The CTI allows a very compact resonator layout which reduces the tank resistance. In comparison to a design with two separate inductors the impedance for common mode signals is significantly smaller. Furthermore, the strong coupling between both inductor parts enhances the signal symmetry which is beneficial for low phase noise.

The oscillator core is a differential emitter coupled type. A capacitive feedback path is used to increase linearity at high swing. Base-emitter junction capacitors of HBT-BJTs are used as varactor diodes. Thus we do not need a biasing network which would have been necessary with base-collector-type varactors. An additional benefit is the shielding provided by the collector which reduces the amount of signal injection into the substrate and vice versa.

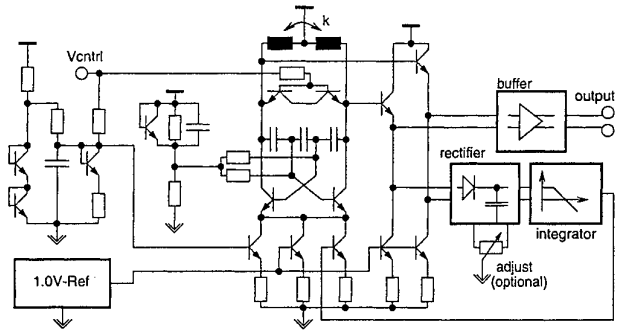

Fig. 1: Oscillator schematic

Biasing of the oscillator is done threefold. Beside a minimum constant current there is an additional current driven by the tuning voltage. This reduces the effect of amplitude modulation due to the reduced varactor quality factor at low reverse voltages. A third current is generated by an amplitude control circuit. This circuit compares the rectified output signal with a reference signal which can be optionally adjusted by an external potentiometer. This regulation significantly reduces the temperature drift as well as the drift over the supply voltage. The measured temperature drift is -700 kHz/K, the measured supply sensitivity is -7.5 MHz/V. With deactivated regulation this value is about one order of magnitude higher. Fig. 2 shows the frequency range over the supply voltage for a regulation area of -2.5 to -3.3 V. With the help of the optional potentiometer this area can be shifted toward lower supply voltages.

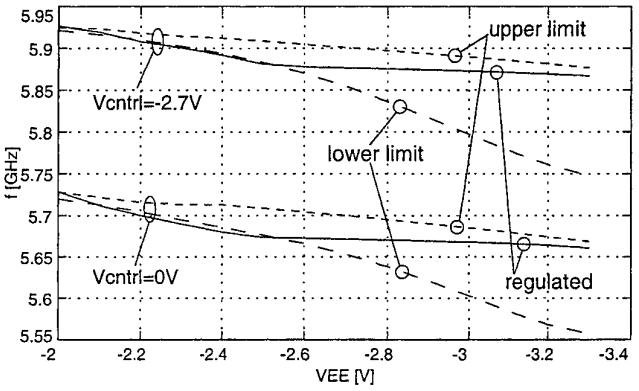

Fig. 2: Effect of amplitude control on VCO frequency

We found that noise contribution from the regulator was

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not well predicted by the simulator. This caused an erratic saving in the blocking capacitor at the regulator output. Actually, the corner frequency at this point should be well below the PLL bandwidth to avoid negative effects on noise.

Getting accurate simulation results requires a precise inductor model. We built a program that generates a distributed model based on a geometrical description of the inductor. This type of model can handle both common- and differential mode as well as RF-effects like skin and proximity over a wide frequency range, thus it is possible to optimize the oscillator without measurement of fabricated inductors.

After a first test [3] with an inductor geometry similar to a previously published one we optimized this circuit based on our modeling tool only. The comparison between simulated and measured data is very good with the exception of the tuning behavior at low varactor voltages, which may result from some inaccuracy of the transistor model. Fig. 3 compares the simulated and the measured curve.

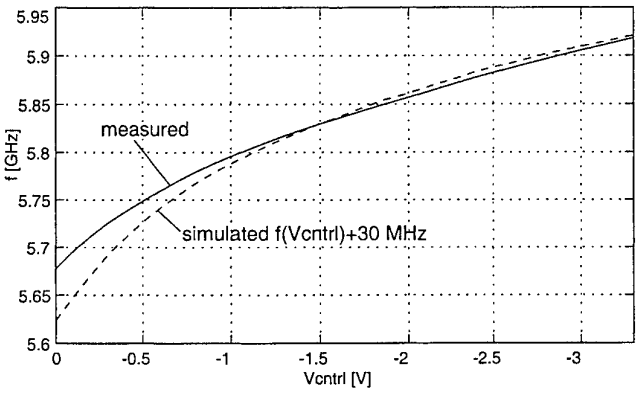

Fig. 3: Oscillator tuning curve

The computed model has an inductance of $2\,x\,0.75$ nH, a coupling of 0.35 and a DC-resistance of $2\,x\,1.0\,\Omega$. A quality factor of 7.4 at 5.8 GHz and a self-resonance at 11.4 GHz is predicted for the three-turn-inductor with 220 μm diameter.

A substrate shield is used to reduce the effect of capacitively coupled substrate currents. This enhances the phase noise by about 3 dB. Fig. 4 shows a chip photo of the oscillator with substrate shield. The active area including bond pads is about $800\,x\,800\,\mu m^2$ large.

IV. Oscillator Measurements

The oscillator is mounted in a CLCC package on a shielded microwave substrate. The measured center frequency of the oscillator is 5.78 GHz, the tuning range is 203 MHz over a control voltage range of 2.7 V (241 MHz over 3.6 V). An SSB phase noise (Fig. 5) of -107 dBc/Hz@1 MHz was measured. The 2^{nd} and 3^{rd} harmonic of the single-ended measured output is at -35 dBc and -48 dBc. The oscillator draws 7.6 mA from a -2.7 V supply, including emitter followers and amplitude regulation, but not including the output buffer. The circuit operates in a supply range of -2.0 to $-3.3\,V$, but at low voltages the output power of the buffer decreases. These results were achieved without special features such as etching or deep trenches.

V. Conclusion

We have presented an integrated 2.7 V VCO for 5.8 GHz WLAN in a low-cost SiGe bipolar technology. Simulations

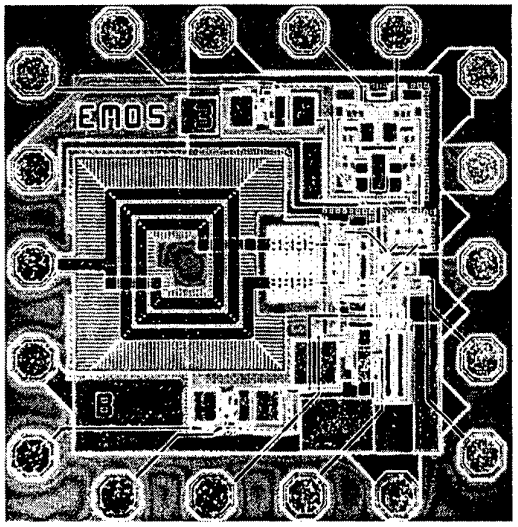

Fig. 4: Oscillator chip photo

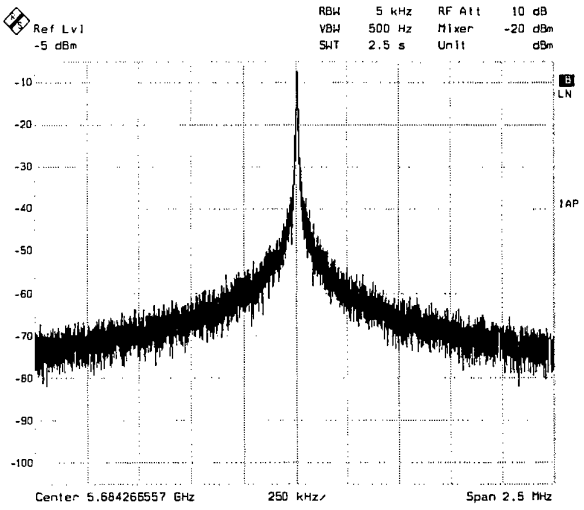

Fig. 5: Free running oscillator spectrum

with a distributed model of the center-tapped inductor are in good agreement with the measurements. Our results demonstrate the suitability of SiGe-HBT for 5 GHz RF circuits.

The authors gratefully acknowledge the fabrication of the experimental IC in a SiGe HBT technology by the IHP in Frankfurt (Oder), Germany. This work was supported by the Bundesministerium für Bildung und Forschung (BMB+F), Germany, under grant 01M2417C0 (project LOTUS II) in the research area on Advanced Microelectronics.

References

[1] Ulf König: 'SiGe & GaAs competitive technologies for RF-applications', *IEEE BCTM 98*, pp. 87-92.

[2] W. Winkler, J. Borngräber, H.B. Erzgräber, H.J. Erzgräber, B. Heineman, D. Knoll, H.J. Osten, M. Pierschel, K. Pressel, P. Schley: 'Wireless Communication Integrated Circuits with CMOS-compatible SiGe HBT Technology Modules', *Proc. CICC 99*, pp. 351-358

[3] G. Grau, U. Langmann, W. Winkler, D. Knoll, J. Osten, K. Pressel: 'A Current-Folded Up-Conversion Mixer and a VCO with Center-Tapped Inductor in a SiGe-HBT Technology for 5 GHz Wireless LAN Applications', *Proc. BCTM 99*, pp. 161-164.

MMIC Power Amplifier Applications of Heterojunction Bipolar Transistors (HBTs)

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Abstract

For the past several years, GaAs based HBT power amplifiers (PAs) have dominated the CDMA handset transmitter market due to their excellent linearity and power added efficiency. Their leading position, however, has been challenged recently by newly emerging IC technologies, such as SiGe HBTs. Compared with GaAs based HBTs, SiGe HBTs are more attractive due to their high substrate thermal conductivity (150W/m-°C), comparable device performance (f_t ~30GHz and f_{max} ~50GHz), lower emitter/base turn-on voltages (~0.75V) and potentially lower production cost. Unfortunately, SiGe HBTs have their own disadvantages: the substrate is conductive, adding significant parasitics to both active and passive components of the power amplifier. SiGe HBTs also have relatively low breakdown voltages (BV_{ceo}~5V; BV_{ces}~14.5V) and low Early voltage (~140V), versus >1000V in GaAs HBTs. These characteristics are detrimental to the gain, linearity and dynamic range of the power amplifier. Recent efforts have demonstrated the use of SiGe HBTs for DECT and GSM handset PA applications. However, the output power of the DECT is relatively low (24dBm) and the linearity requirement of the GSM is far less restrictive than that of the CDMA. To make a fair comparison of GaAs and SiGe HBTs for power amplification applications, we have designed and characterized a SiGe HBT MMIC PA for dual mode (CDMA/AMPS) cellular handset applications.

We use a two-stage amplifier configuration to fulfill the dual-mode design goals. A simplified schematic is shown in Fig.1, which comprises driver and power stages, input, interstage and output matching networks and bias circuits for the driver and power stages, respectively. To design a power amplifier with both high linearity and high PAE, we use an RC feedback network to linearize the 1st stage and bias the 2nd stage at a rather low quiescent point to trade for high PAE. In the micro-module, two microwave transmission lines, TRL1 and TRL2, are implemented on alumina substrate to transform low output impedance of the 2nd stage power HBT to the standard 50Ω output. Harmonic tuning techniques are also employed to suppress the second and third harmonics at the output by using shunt resonators made of microwave transmission lines (TRL3 and TRL4) in series with shunt capacitors. TRL3 is designed to resonate with a serial capacitor C2 to reflect the 2nd harmonic signal. TRL4 is designed to resonate with the capacitor C3 to reflect the 3rd harmonic signal. Since primary harmonic components are mostly eliminated from the amplifier output, the linearity and efficiency of the PA are significantly enhanced.

The designed power amplifier satisfies both CDMA and AMPS requirements in output power, linearity and efficiency. At V_{cc} =3V, the power amplifier shows excellent linearity (1st ACPR < -44.1dBc and 2nd ACPR < -57.1dBc) up to 28dBm for CDMA applications (Figs 2). Under the same bias conditions, the PA also meets AMPS handset requirements in output power (up to 31 dBm) (Fig.5) and linearity (with 2nd and 3rd harmonic to fundamental ratios lower than –37 dBc and –55 dBc, respectively) (Fig.6). At the maximum output power level, the worst power-added-efficiencies (PAE) are measured to be 36% for CDMA (Fig.3) and 49% for AMPS operations (Fig.5).

The above measured performance is comparable to that of GaAs HBTs but with two exceptions: 1) SiGe HBT PAs show a relatively low gain than that of GaAs HBTs (about 4-6dB as shown in Figs.4 & 7). This may be attributed to the use of low-Q on-chip inductors (Q<5) in matching networks and more difficult modeling of SiGe devices and interconnect parasitics at high frequencies; 2) SiGe PAs survive severe output mismatch (VSWR >12:1) up to V_{cc}=4V but die instantly as V_{cc} >4.5V, due to its low breakdown voltages. We also observe high inter-modulation spurs (-22dBc) appeared in CDMA outputs at two specific tuning angles, as shown in Fig.8, but no spurs appeared in AMPS outputs. The possible mechanism of generating those spurs will also be discussed during the talk.

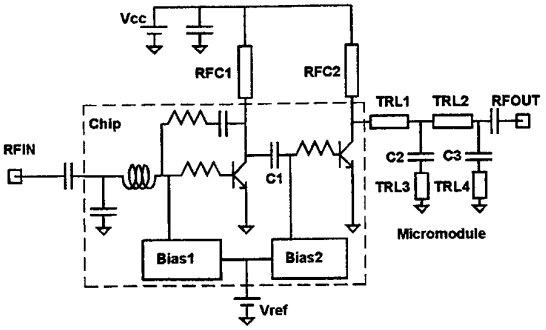

Fig. 1

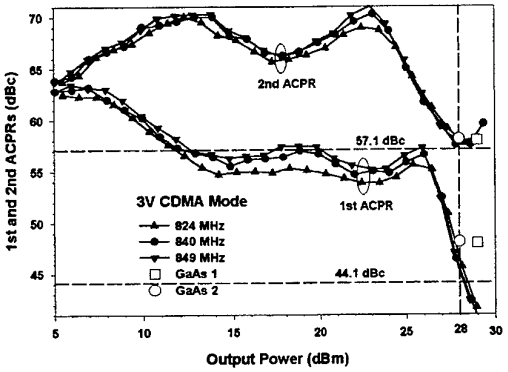

Fig. 2

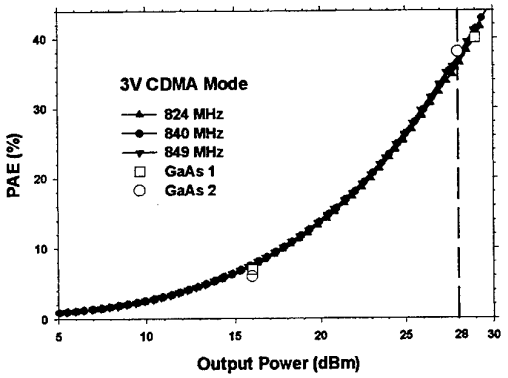

Fig. 3

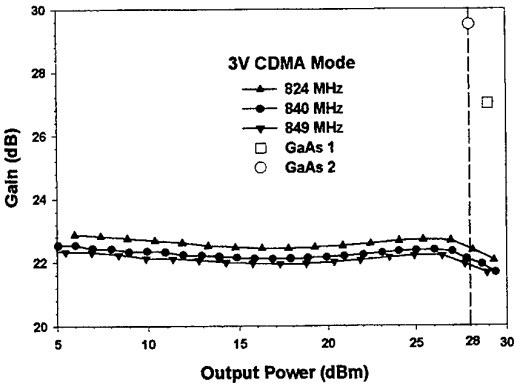

Fig. 4

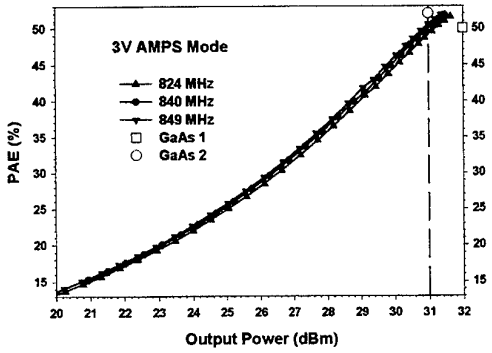

Fig. 5

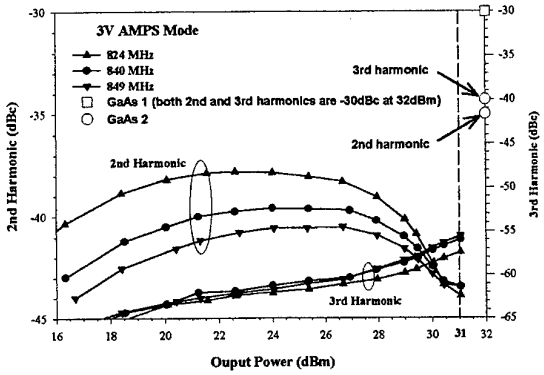

Fig. 6

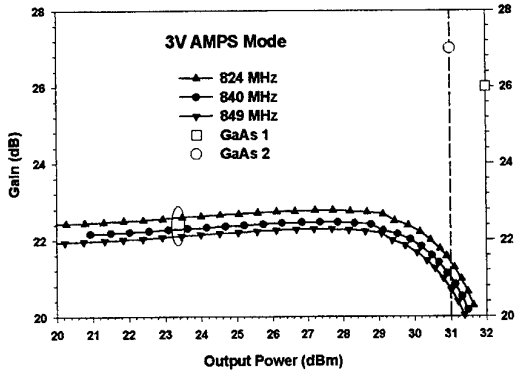

Fig. 7

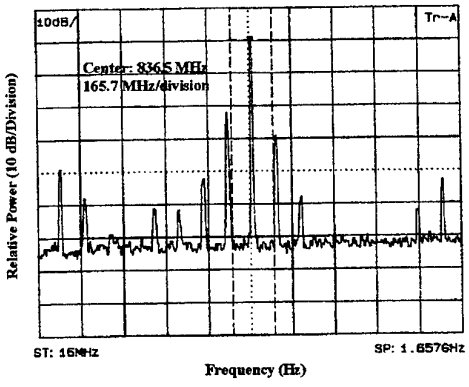

Fig. 8

Potential of SiGe Heterostructure FETs for Micropower Applications

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Introduction: As industry moves towards higher integration and lower cost for wireless and video products there is an overwhelming demand for micro-power technology. New, low-power wireless telecommunications and medical devices such as "wearables" are placing significant demands upon the power consumption of ICs. Furthermore devices and systems are finding that audio, base band and even IF processors are demanding significantly lower power consumption if standby time levels are to be increased. So far the micro-power revolution has taken off in applications such as hearing aids and other medical devices. An important area of potential application of SiGe circuits is the weak inversion region. Traditionally, the weak inversion region of operation has been reserved for medical applications. Use of weak inversion circuits in high frequency applications has been avoided for a couple of reasons. The frequency of operation of transistors in subthreshold is limited due to the picoamp current levels, and in silicon short channel affects appear to undermine subthreshoild operation at gate lengths below about 1 micron. In contrast to the digital approach, where a single operation is performed by a series of switched on or off devices, *the physics of the elementary device itself can be exploited to perform the same operation in an analogue way*; hence the energy per unit computation is lowered and power efficiency is increased [1]. In this paper we explore the potential of SiGe to realise micropower circuits, by exploiting the higher electron mobility to realize micropower circuits which operate at much higher frequency than is possible with standard silicon CMOS.

Technology: Most of the work on Si:SiGe MOS and Schottky gated heterostructures has concentrated on short channel length and high frequency applications[2]. Interest in low power applications of SiGe devices has been concentrated on heterojunction bipolar transistors (HBT). Recently the interest in micropower applications using SiGe MOS has increased in view of current work using silicon mosfets [3]. Although this mobility enhancement has not yet been confirmed experimentally, we have already shown a three times increase in threshold mobility in n-channel depletion mode SiGe FETs compared to Si MOSFETs, while operating in the subthreshold region . These findings do not only make n-channel SiGe FETs interesting for micropower but also for CMOS applications. This mobility enhancement of SiGe devices should increase f_T by an order of magnitude, pushing lowpower applications into the video frequency range. Bipolar Junction Transistors (BJTs) are characterized by higher transconductance value g_m and generally higher transition frequency f_T when compared to MOSFETs. Modern bipolar processes are reliably characterised for collector current levels as low as 10-100pA enabling -in principle- micropower operation. However, high integration density demands in conjunction with the necessity for compact single-chip (possibly mixed-mode) solutions render the MOSFET the natural candidate for the design of analogue VLSI micropowered circuits. When weakly-inverted, MOSFETs are characterised by diffusing carrier flow. This region is characterised by drain current levels ranging typically from 1pA to 10nA. Thus, the exploitation of weakly-inverted MOSFETs powered by low (~3V) power-supply voltages leads readily to the realisation of analogue micropowered designs.

Generally, MOSFET devices when weakly-inverted are governed by an exponential V-I characteristic (dictated at carrier level by the Fermi-Dirac distribution function):

$$I_{DS} = I_{n0}\left(\frac{W}{L}\right)\exp\left[\frac{V_{GS}}{nV_T}\right]$$

I_{n0} is a process-dependent constant with typical values of a few nAs, n denotes the subthreshold slope factor (typically between 1.5-2) and W/L is the device aspect ratio.. The choice of subthreshold region operation is consistent with the design principle of speed maximisation per unit power consumed. The ratio of the achievable speed over the necessary power is a measure of the efficient use of the available power; this "figure of merit" is maximised when the drive capability g_m/I of the device is maximised. The quantity g_m/I exhibits its maximum value when the device is weakly-inverted constituting the subthreshold operation region of the MOS transistor. Additionally, high g_m/I values lead to reduced voltage swings which minimise the current wasted for the charging and the discharging of parasitic capacitances allowing the use of smaller current signals which, in turn, reduce the quiescent power consumprion. The Current-Mode approach [4] enables the design of high dynamic range systems since signals are represented by currents: junction leakage currents and noise constitute the lower signal limit, whereas degraded g_m/I values and distortion constitute the upper signal limit.

Typically, four decades of current signal levels can be accommodated within the weak-inversion region

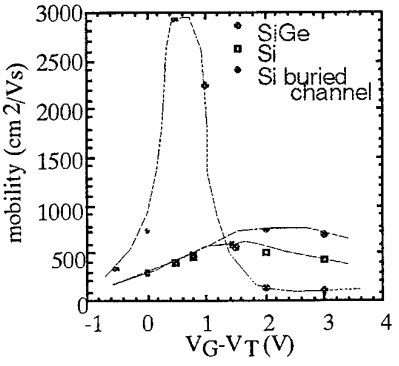

Figure 1 Intrinsic mobility comparison

Device and Circuit characterisation:

We have successfully fabricated n-channel depletion-mode (d-mode) SiGe heterojunction MOSFETs (HMOS). Extrinsic characteristics were non-ideal due to large parallel conduction in the supply layer and large contact resistances (300Ω). The device characteristics are: - Gate length l_g=3μm, width W_g=200μm, oxide thickness t_{ox}=15nm- Threshold voltage V_T=-1.8V, interface state density

Q_{it}=5 10^{11} cm^{-2} - DC transconductance g_m^{max}=41mS/mm - AC transconductance and cut-off frequency: f_T=25 MHz with g_m^{max}=1 mS/mm above threshold. - The sub-threshold slope is 100mV/dec.

The intrinsic mobility (mobility value corrected for the high series resistance) as a function of gate voltage is given in Figure.1. The mobility improvement in our non-optimised devices in comparison to Si MOSFET is obvious. Note the improvement of mobility around threshold by 3 times, illustrating the promise of SiGe micro power circuits. Low temperature device measurements (77K) have shown a 7 times improved g_m at low drain voltages and a 3 times reduced leakage current, making SiGe MOS extremely interesting for low temperature applications. The successful devices have been used to build an inverting current mirror with cross-coupled gates [6]. The circuit functioned well, above threshold, though leakage currents were too large for good sub-threshold operation. A mask has been developed to repeat these measurements on a monolithically integrated circuit and results should be available for the conference

Circuit Techniques: The aim of this paper is to demonstrate simple analogue SiGe nMOS and CMOS circuit techniques to realise micropower building blocks such as current mirrors, linear transconductors, differential-pairs and mixers using SiGe devices. One of the main blocks investigated so is the current mirror both in NMOS and CMOS (see Figure 3). More complex circuits such as amplifiers, folded cascode structures and mixer cells will be presented and used to overcome problems related to non-optimised device structures for sub-threshold operation. The current-level dependence of the FET drive capability g_m/I exhibits a maximum when the device is weakly inverted. The current-mode approach developed by Toumazou [5] enables the design of high dynamic range systems since signals are represented by currents: junction leakage current and noise constitutes the lower signal limit, whereas degraded g_m/I values and distortion constitute the upper signal limit. Due to the improved linearity of the SiGe circuits distortion is expected to happen at higher frequency. At transistor level classic linearisation schemes (e.g. resistor degeneration, device cross-coupling and sizing, etc.) suitable for the MOSFETs can be directly applied. Recently however, novel current-mode design techniques have been invented. These techniques, widely referred to as "log-domain" [4], directly exploit the non-linear (exponential) V-I characteristic of an active device to achieve increased dynamic range. Even though each individual device non-linearity is exercised strongly, an ensemble of appropriately interconnected transistors can lead to the systematic formation of externally-linear-internally-non-linear signal processors. Such processors are, for example, suitable for the construction of linear time-invariant frequency shaping networks.

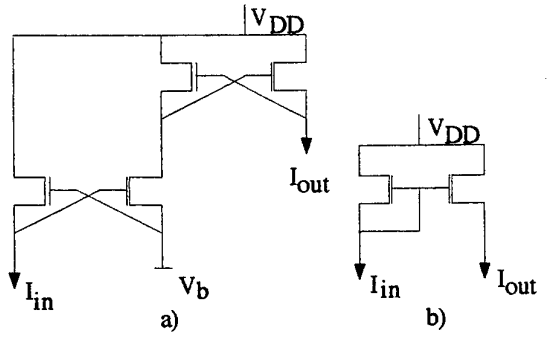

Figure 3: Linear current mirror a) NMOS , b) CMOS

As an example of our previous work, Figure 4 illustrates a practical fully-tunable biquadratic micro-power filter for a cochlea implant, designed at Imperial College and fabricated with a 0.6micron CMOS technology in collaboration with Northern Telecom [4]. Figure 5 illustrates the corresponding mask layout indicating the compact dimensions of this analogue solution. The measured frequency responses shown in Figure 6 represent state-of-the-art performance; the total power consumption is lower than 1μW (i.e. an enviable 250nW/pole. The filter cut-off frequency is tunable from 100Hz to 10KHz. In the paper we will present a similar design operating over a broader frequency range using SiGe technology to demonstrate the potential of this promising technology.

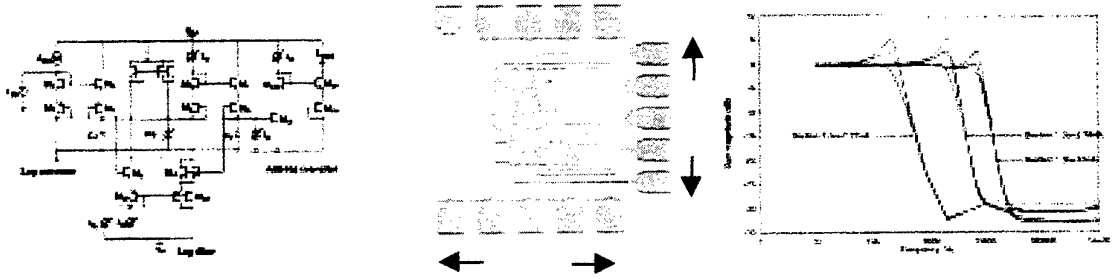

Figure 5 Filter mask

References

[1] C.Mead, "Neuromorphic Electronic Systems", Proceedings of the IEEE, vol.78, no.10, pp.1629-1636, 1990

[2] U. Konig, M. Zeuner, G. Hock, T. Hackbarth, M. Gluck, T. Ostermann, and M. Saxarra, "N- and p-type SiGe HFETs and circuits", Solid State Electron. 43, 1383, (1999)

[3] C.Toumazou, J.Ngarnmil and T.S.Lande, "Micropower log-domain filter for electronic cochlea", Electronics Letters 30(22), (1994).

[4]J.Ngarnmil, C.Toumazou and T.S.Lande, "A fully tuneable micropower log-domain filter", 2nd European Solid State Circuit Conference, ESSIRC'95, France, 1995

[5] C. Toumazou, F.J. Lidgey, and D.G. Haigh,-book "Analogue IC design: the current-mode approach",UK, IEE , 1990

[6] K. Fobelets, W. Jeamsaksiri, J. Hampson, C. Toumazou, and T.Thornton, "Si:SiGe MODFET current mirror", Electron.Lett. 34(22) 2076 (1998)

Advanced SOI-MOSFETs with Strained-Si/SiGe Heterostructures (Invited)

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I. Introduction

Thin-film SOI structure is a candidate for sub-100 nm devices, because of high carrier mobility for its low channel impurity concentration, low parasitic capacitance of source/drain junction, and simple isolation [1]. However, the carrier mobility of Si channel, particularly, the hole mobility, is not sufficiently high, resulting in limiting the progress of switching speed of CMOS devices. Thus, strained-Si MOSFET is one of a promising device structure for scaled high speed and low power CMOS, because of high electron [2] and hole mobility [3] in the inversion layer. The mobility in strain-Si MOSFETs increases with an increase in strain determined by the Ge content of SiGe layer beneath the strained-Si film.

In this paper, we propose a new strained-Si device structure, n- and p-MOSFETs on strained-Si-channel/SiGe-on-Insulator substrate (strained-SOI). We demonstrate high quality of the strained-Si layers and higher electron/hole mobility of strained-SOI devices [4], [5].

II. Strained-SOI Substrate

A key factor to realize strained-SOI n- and p-MOSFETs shown in Fig.1 is the fabrication of a SiGe layer on a insulating layer by SIMOX technology [6] and the re-growth of a high-quality strained-Si film on this relaxed-SiGe film [7]. The fabrication steps are shown in Fig. 2. First, conventional relaxed and low Ge content 1st-$Si_{0.9}Ge_{0.1}$/graded SiGe buffer layers with 1.8 μm thick were grown, using a UHV-CVD reactor, considering of the trade-off in the SIMOX annealing temperature between the melting point of SiGe films and the formation of high-quality buried oxides [8]. Next, oxygen ions (180 keV, 4×10^{17} cm^{-3}) were implanted into the relaxed $Si_{0.9}Ge_{0.1}$ layer, followed by high temperature annealing (1350 °C for 6 hours) to grow a buried SiO_2 layer inside the $Si_{0.9}Ge_{0.1}$ layer. After that, a 2nd-$Si_{1-x2}Ge_{x2}$ layer and a 20 nm thick strained Si layer were re-grown on this substrate. In this study, the Ge content of 2nd-SiGe layer x_2 was 0.1 in n-MOS, and in p-MOS, x_2 was varied from 0.1 to 0.2.

It is found from TEM observation shown in Fig. 3 that buried oxide of 100 nm with flat interfaces is formed inside a $Si_{0.9}Ge_{0.1}$ buffer layer. Strained-SOI thickness is 340 nm. As shown in Fig.4, the EDX data reveal that the buried oxide is composed of SiO_2 including little Ge atoms and that the Ge content of the SiGe layer on the buried oxide is kept to be 10 %, although the Ge content under the buried-oxide is lower than 10%, because of the Ge diffusion during the SIMOX anealing. The successful fabrication of SiGe layer on SiO_2 is attributable to the block of the diffusion of Ge atoms by buried oxides, meaning the superiority of the SIMOX technology. Also, according to Fig.5, in the case of x_2=0.1, it is confirmed from Raman spectroscopy [8] that a top Si layer has tensile strain induced by fully relaxed $Si_{0.9}Ge_{0.1}$ substrates. In the case of x_2=0.2, the Raman shift of the SiGe layer was almost equal to that in SiGe with the Ge content of 0.135. This fact is explainable by both the stress relaxation of 2nd-SiGe due to the dislocation absorber of the 1st-SiGe and the stress balance between the compressive strain of the 1st-SiGe and the tensile strain of the 2nd-SiGe. It is found, in addition, from AFM images shown in Fig. 6 that the cross-hatched pattern disappears in strained-SOI structure. This smoothing of the surface, attributable to the re-crystallization of SiGe during the high temperature annealing in the SIMOX process, is profitable to the improvement of the device fabrication process and the device reliability. It is concluded from these results that the SIMOX technology, which allows to provide much thinner relaxed-SiGe layers on insulator (< a few 10 nm) for ultra-thin strained-SOI structure, is suitable for the device fabrication on this structure.

Fig. 7 shows that the breakdown voltage of the buried-oxide film in strained-SOI structure was about 10 V. It is possible to further improve this breakdown voltage by optimizing the SIMOX process

The gate oxide of 9 nm thick was grown by thermal oxidation at 800°C. Single n^+ and p^+ drain structures were formed by As^+ and BF_2^+ ion implantation, respectively. Conventional SOI MOSFETs using the usual SIMOX wafer were also fabricated by the same FET process steps.

III. Results and Discussion

A. Drain Current Characteristics

Fig.8 shows the typical drain electron and hole current characteristics of strained- and control-SOI MOSFETs, where L_{eff} are around 10 μm. It is clear that good drain current characteristics were obtained in strained-SOI n- and p-MOSFETs. Moreover, the drain currents of both n- and p-MOS are enhanced in the strained-SOI devices, which is due to the carrier mobility enhancement, as mentioned in the next section. Fig.9 also indicates I-V characteristics in the triode region of n- and p-channel strained-SOI MOSFETs, confirming the normal FET operation, though the drain leakage currents were observed, probably because of residual defects which can be reduced by optimizing the SIMOX process.

Fig.10 shows the typical G_m characteristics of both strained- and control-SOI MOSFETs. It is found that G_m of both n- and p-channel MOSFETs is larger in strained-SOI MOSFETs than that in the control-SOI devices. The enhancement of G_m in n-MOSFETs is much larger, because of the significant mobility enhancement for electrons at low Ge content, theoretically predicted [9]-[11]. On the other hand, the G_m enhancement of p-MOSFETs is found to increase with increasing the Ge content of the 2nd-SiGe. The hump in G_m in p-MOS with x=0.18, observed near Vg of −0.6 V, is attributable to the hole current in the buried channel at the strained-Si/SiGe interface, where the valence band discontinuity of ~0.1V exists.

B. Electron/Hole Mobility Enhancement

Electron and hole mobility behaviors are shown in Fig. 11. The carrier mobility was obtained for MOSFETs with W_{eff}/L_{eff} of 100 μm, by dividing I_d at $|V_d|$ of 5 mV by the carrier density in the channel. It is found that electron mobility in strained-SOI MOSFETs are significantly enhanced, compared to the universal mobility of Si bulk-MOSFETs [12] and the control-SOI MOSFETs, in addition to the hole mobility. At E_{eff} of 0.1 MV/cm, the enhancement factors of the electron and the hole mobility against the universal mobility are 1.6 and 1.3 at x_2 of 0.2 (1.05 at x_2 of 0.1) in strained-SOI MOSFETs, respectively. Also, when compared to the control-SOI MOSFETs, the hole mobility in strained-SOI are larger by 1.45 at x_2 of 0.2 (1.18 at x_2 of 0.1). Consequently, it is found that, with increasing the Ge content of SiGe layer beneath the strained-Si from 0.1 to 0.2, this is, increasing the tensile strain of the strained-Si, the enhancement factor of the hole mobility increases from 1.05 [1] to 1.30.

IV. Conclusion

We have proposed and successfully fabricated n-and p-channel advanced SOI MOSFETs with strained-Si channel formed by the combination of SIMOX and high quality strained-Si re-growth technologies. We have demonstrated both electron (60%) and hole (30%) mobility enhancement in the strained-SOI MOSFETs, compared to both the universal carrier mobility and the control-SOI MOSFETs. Furthermore, strained SOI p-MOSFETs using double-layered $Si_{0.8}Ge_{0.2}/Si_{0.9}Ge_{0.1}$ structure was proposed. This device was shown for much higher hole mobility.

Acknowledgment

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References

[1] M. Yoshimi et al., **ED-44**(1997)423. [2] J. Welser et al., **EDL-15**(1994)100 [3] K. Rim et al., IEDM Tech. Dig. (1995)517 [4]T.Mizuno et al., IEDM, p. 934 (1999). [5] T.Mizuno et al., Symp. VLSI Tech. (2000). [6] S. Fukatsu et al., Appl. Phys. Lett., **72**(1998)3485. [7]N.Sugiyama et al., Int. Joint Conf. Si Epitaxy and Hetrostrucrure, E-3 (1999) [8] Y. Ishikawa et al., Appl. Phys. Lett., **75**, 983 (1999).. [9] R.Oberhuber et al., Phys.Rev., **B58** (1998) 9941 [10] M. Rashed et al., IEDM., p. 765 (1995). [11] S.Takagi el al., J.Appl.Phys., **80**, 1567 (1996).[12] S.Takagi et al., **ED-41**, 2357 (1994).

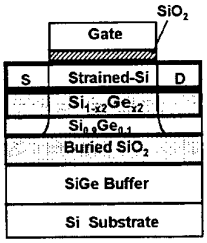


Fig.1 Schematic cross section of strained-SOI MOSFETs. x_2 of nMOS was 0.1, and in the case of pMOS x_2 was varied from 0.1 to 0.2.

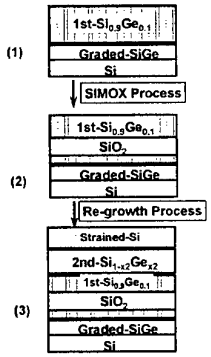


Fig.2 Process steps of strained-SOI substrate by SIMOX and re-growth technique of strained-Si and 2nd-SiGe layers.

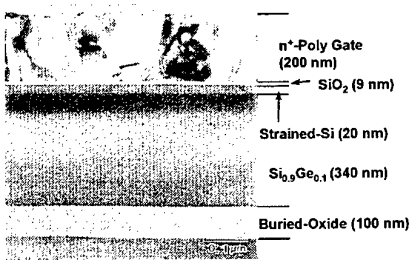


Fig.3 TEM photograph of cross section of strained-SOI MOSFETs with 2nd-$Si_{0.9}Ge_{0.1}$ layer. Uniform buried oxide and strained-Si were fabricated.

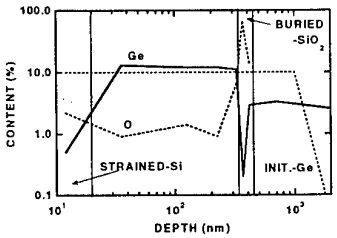


Fig. 4 EDX data of Ge and O contents in strained-SOI substrate with $Si_{0.9}Ge_{0.1}$ layer. Ge content of SiGe layer on the buried oxide is uniform and about 10%, while the Ge content under the buried oxide is lower.

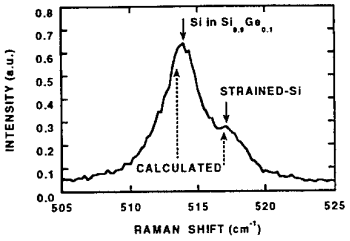


Fig.5 Raman shift of both strained-Si and relaxed-SiGe layers at x=0.1. Both shifts are almost the same as the calculated ones.

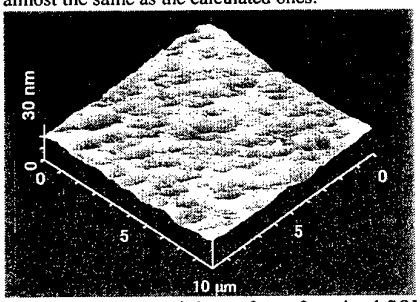


Fig.6 AFM image of the surface of strained-SOI substrate with x_2=0.1. The cross-hatch pattern disappeared.

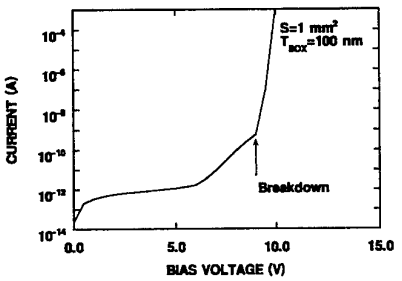
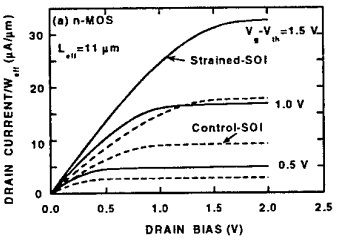


Fig.7 Breakdown characteristics of buried oxide with I mm^2 area. The breakdown voltage is about 10 V.



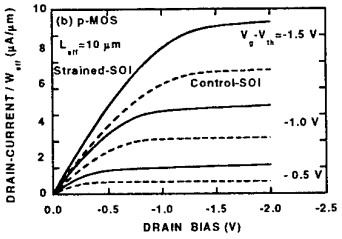


Fig.8 Drain current characteristics of strained- (solid lines) and control-SOI (dashed lines) devices, where W=5μm. (a) nMOS, and (b) pMOS with x_2=0.1. Good I_d characteristics are obtained in strained-SOI. In addition, I_d of strained-SOI MOSFETs are enhanced, compared to that of control-SOI devices

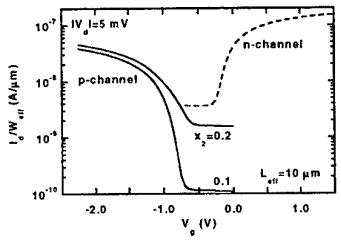
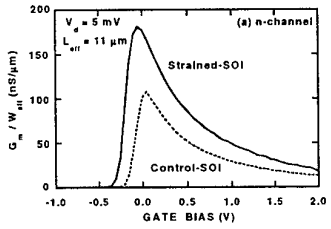


Fig.9 Triode I-V characteristics of both n- (dashed line) and p- (solid line) strained-SOI MOSFETs at L_{eff}=10 μm and $|V_d|$=5 mV. Normal FET operation was obtained in both channels, whereas somewhat leakage currents were observed.



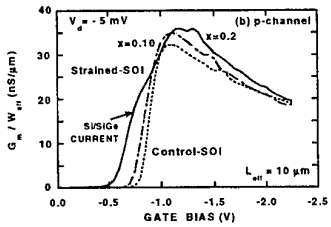
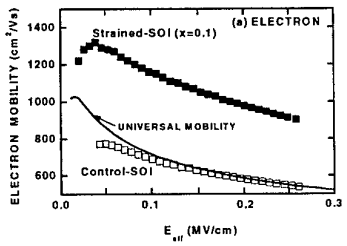


Fig.10 Typical transconductance behavior at $|V_d|$=5 mV of both strained- and control-SOI (dashed lines) MOSFETs. (a) n- and (b) p-channel. G_m of strained-SOI MOSFETs is enhanced in both channels and G_m of p-MOS increases with increasing the Ge content of 2nd-SiGe layer.



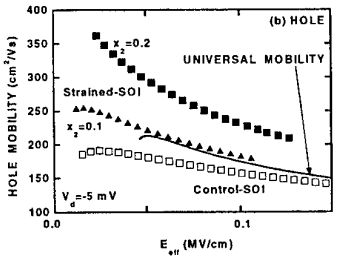


Fig.11 (a) Electron and (b) hole mobility vs. E_{eff}. The solid line shows the universal mobility of Si-bulk MOSFETs [12]. Mobility is enhanced in strained-SOI MOSFETs, compared to both the universal mobility and that of control-SOI devices. Hole mobility increases with increasing x_2.

Silicon-based Technologies for Wireless: A Value-added Approach

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Within five years, mobile communication and internet will be submerged into a technology offering location- and context-aware, person-specific information and services, "on the fly" to the mobile individual, "untethered" to the desk-bound. The "global village", defined by today's wired internet, will blossom into local wireless worlds, each offering the information and services available (and appropriate) at that location. At the Louvre, your "Chameleon Access Device" will download its personality from the "local ether" to purchase you a ticket as you enter, guide you to the Rubens or the da Vinci sections, and inform you about the 9Mona Lisa as you stroll past it. It will show you the location of the nearest Creperie as you leave, help you find a taxi, and, should you wish, inform your spouse of your whereabouts.

The Table summarizes the technical demands of "Chameleon Technologies" compared with what is currently possible today. In short, a $99 device is needed, whose primary value resides in a single chip, or at most very few chips, with broadband wireless and advanced information processing capabilities.

This prospect, driven by the astonishing growth of the communication market, has caused a major revolution in the silicon industry. Communication has now taken over from the microprocessor as the key driver, just as the microprocessor superceded memory 15 years ago. To first order, communication will be silicon-based, and single-chip.

A single-chip chameleon engine will consist of ~10M CMOS "baseband" digital gates, and ~100k "frontend" analog components, including transistors, and integrated filters and directional antennas. The analog transistors will consist of CMOS and bipolar. The exact mix between CMOS and bipolar will be decided by cost, including first-pass design capability and time-to-market. It seems unlikely that a purely CMOS or silicon homobipolar solution will suffice. The most prudent current bet for the wireless frontend of the future involves a Si CMOS+SiGe HBT mixture.

The digital baseband will be implemented using existing cores, augmented with integrated, IP-based "communication accelerators" (just as the 486 microprocessor featured a 386 "core", augmented with an integrated floating-point accelerator). The frontend solution will be based on new analog "cores", implemented specifically for the analog (CMOS and HBT) processes at hand. Re-use of existing digital baseband cores in single-chip wireless engines with analog capability implies that the analog devices must be added in a strictly "modular fashion", with no changes to the digital device characteristics. Cost-effectiveness means, in addition, that such modules must be simple, and high performance, and involve no changes to the digital CMOS process or process flow.

These considerations have stimulated work at system, circuit, and process technology levels. At system level, "communication accelerator" cores and protocols are under development, which allow existing cores (DSPs / microprocessors / microcontrollers) to perform important communication functions, particularly those based on the IP protocol. At circuit level, efforts are under way to develop RF "macro libraries" that implement key circuit blocks in specific

analog-capable Si-based process modules. At technology level, CMOS-compatible, modular processes have been developed, which combine high performance with intrinsic simplicity, and hence low cost. At each level, the proposed solution builds on an existing mainstream silicon solution, thus adding value to it. This is the most promising means of dealing with silicon; joining it, rather than attempting to beat it.

Valuable as these developments are, the key technical challenge lies in integrating these capabilities at system, circuit, and process technology levels into a single-chip chameleon engine costing less than $10.

The social challenge of dealing with location- and person-aware chameleon technologies is beyond the scope of this presentation.

Mobile Access Devices: Now and the Future

Attribute	**Now**	**Needed**	**Challenges**
Bandwidth	9.6 kb/s	20 – 50 Mb/s	1000x improvement
Processing	100 MIPS	10,000 MIPS	100x improvement
Power consumption	1 mW/MIPS	0.01 mW/MIPS (effective)	100x improvement
No. of chips	10 – 50 chips (@9.6 kb/s)	1 chip (@20 Mb/s)	Not possible at present
Form factor	Brick	Distributed	Internal communication, power distribution, packaging
Software	Win CE or Palm Pilot	Java / Jini	HW-independent
Services	Voice (+ a little data)	Transaction + data + voice	Integrated, seamless, secure
Features	Undifferentiated	Location-, context-, person-aware	"Chameleon" capability
Cost	$299	$99	Margin too low for service-based purchase of access device

Acknowledgments: I have benefited greatly from discussions with colleagues at the *IHP* and *lesswire AG*, whose work forms the basis of this presentation.

High-Speed SiGe HBT ICs for Optical Receivers

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The ICs for 40-Gb/s optical transmission systems must be capable of operation at that bit-rate, but must also be sufficiently inexpensive for wide-spread commercial use. Because of its high speed and high level of integration, the SiGe heterojunction bipolar transistor (SiGe HBT) is an attractive low-cost candidate for such an application. To realize a 40-Gb/s optical receiver (Fig. 1), we have developed a 0.2-μm self-aligned selective-epitaxial-growth (SEG) SiGe HBT and have designed and fabricated a wide-bandwidth preamplifier, a high-gain limiting amplifier, and a 1:4 demultiplexer with a bit-rotation function.[1,2]

An SEM cross-sectional view of a 0.2-μm self-aligned SEG SiGe HBT is shown in Fig. 2. To provide a good link between the intrinsic and extrinsic base, we introduced a poly-Si-assisted self-aligned SEG (PASS) structure. The PASS structure enabled both low base resistance and low collector capacitance. Shallow-trench (0.4 μm deep) and dual 0.6-μm-wide deep-trench (3 μm deep) isolations were used to reduce the parasitic capacitance of the collector and substrate. Table 1 shows typical transistor parameters. The peak cut-off frequency (f_T) and the peak maximum oscillation frequency (f_{max}), for a SiGe HBT with a 0.2 x 1.0 μm emitter area at a collector-to-emitter bias voltage of 2 V, were 105 GHz and 140 GHz, respectively, at a collector current density of 7.5 mA/μm^2.

Figure 3 shows a schematic of a preamplifier. For practical use, a wide bandwidth of over 40 GHz is needed to ensure the total bandwidth is more than 30 GHz with the AGC amplifier and decision circuit even when the input capacitance Cin is as high as 100 fF and fluctuating. To improve the bandwidth, we introduced a common-base input stage (CBIS) in front of a conventional transimpedance amplifier.[3] The CBIS also reduces the effect of Cin on the frequency response, and thus allows us to use a high input-capacitance photodiode. The V_{RL} bias circuit provides stable voltage for load resistor R_L, and can be designed flexibly. This reduces the effect of supply-voltage deviation on circuit performance. We calculated the transimpedance gain from measured S-parameters, taking Cin into account (Fig. 4). A bandwidth of 45 GHz was obtained with a transimpedance gain of 50 dBΩ when Cin was 100 fF.

Figure 5 shows a block diagram of a limiting amplifier and a schematic of an amplifier stage. A high gain at 40 GHz is required to generate a clock signal with a constant voltage swing for a decision circuit and a demultiplexer. In an amplifier stage, a differential transimpedance amplifier is used as an active load to increase the bandwidth.[4] Moreover, to increase the gain at 40 GHz, we used gain peaking by using two emitter follower stages. Biasing resistors R_{bias} were used to prevent transistor Q_F operating in the cut-off region. The measured minimum saturation input was -30 dBm at 40 GHz; low enough for a 40-Gb/s system. A 500-mV_{pp} output-voltage waveform with little distortion was made possible by the biasing resistors (Fig. 6).

We also integrated a decision circuit and a 1:4 demultiplexer, and included a circuit for the bit-rotation function,[5] in a single chip. The bit-rotation function is needed to assign the data to each output port. This integration reduces the total power consumption. We successfully obtained well-opened eye diagrams at a data rate of 40 Gb/s.

In summary, we have developed high-speed ICs for a 40-Gb/s optical receiver based on SiGe HBTs. We obtained excellent results that met the IC requirements for a practical 40-Gb/s optical receiver, and provide an adequate margin for any performance degradation caused by packaging. Therefore, by using SiGe HBT technology, we will be able to provide all the ICs needed for a 40-Gb/s optical receiver, and these ICs will provide high reliability at a reasonable cost.

References

[1] K. Washio et al., IEEE IEDM, Dig. Tech. Papers, 1999, pp.557-560.
[2] T. Masuda et al., IEEE ISSCC, Dig. Tech. Papers, 2000, pp.60-61.
[3] T. Vanisri et al., IEEE Journal of Solid-State Circuits, vol. 30, No. 6, pp. 677-685, June 1995.
[4] M. Moller et al., IEEE Journal of Solid-State Circuits, vol. 29, No. 7, pp. 815-822, July 1994.
[5] Z. Lao et al., IEEE Journal of Solid-State Circuits, vol. 31, No. 1, pp. 54-60, January 1996.

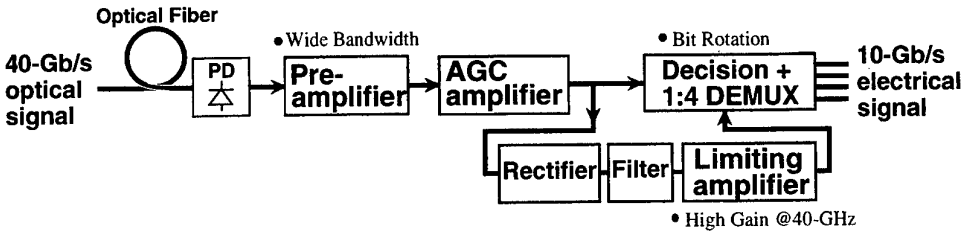

Fig. 1. Block diagram of a 40-Gb/s optical receiver.

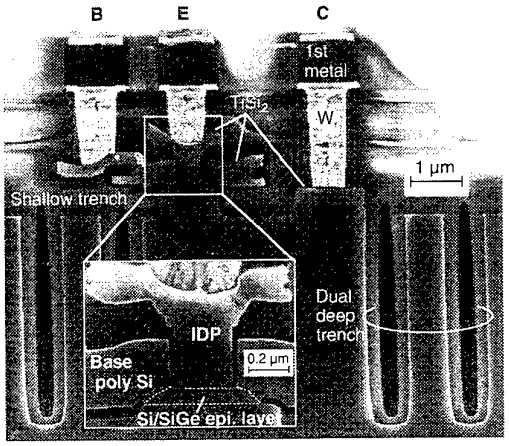

Fig. 2. SEM cross-sectional view of a 0.2-μm SiGe HBT.

Table 1. Typical transistor parameters.

A_E = 0.2 x 1.0 μm		
h_{FE}	1600	
BV_{CER}	3.0	V
R_E	33	Ω
R_B	180	Ω
C_{jC}	2.0	fF
C_{SUB}	1.6	fF
f_T	105	GHz
f_{max}	140	GHz

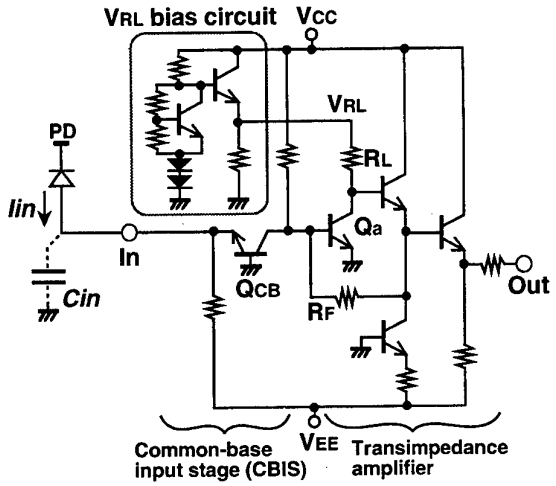

Fig. 3. Schematic of a preamplifier.

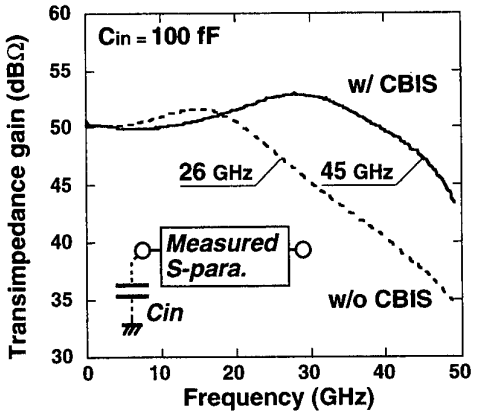

Fig. 4. Frequency response of transimpedance gain.

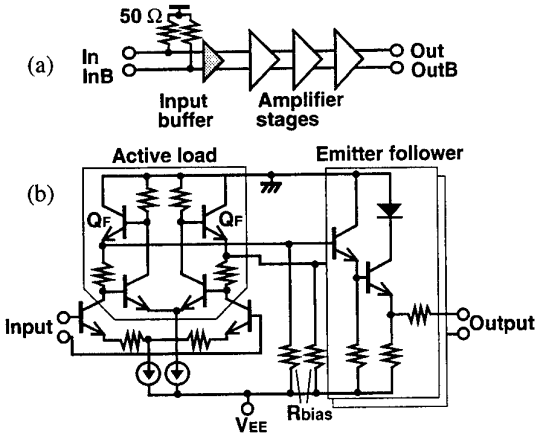

Fig. 5. (a) Block diagram of a limiting amplifier, (b) Schematic of an amplifier stage.

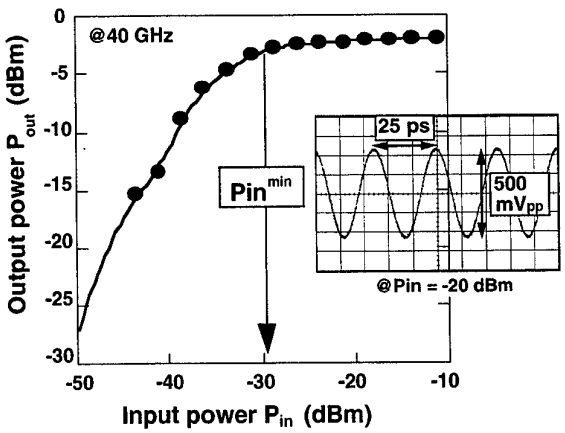

Fig. 6. Output characteristics of a limiting amplifier.

SiGe-HBTs for Bipolar and BICMOS-Applications: From research to ramp up of production

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SiGe technology is a favorite candidate for high frequency applications, especially for the emerging market of wireless communication, because it satisfies the need for high performance and the reduction of system costs by highly integrated circuits. Selective epitaxy of SiGe/Si layer systems in praticular allows a completely self- aligned process and enables a simple control of the epitaxial growth.

The process flow starts with a p-doped substrate, implantation and diffusion of a highly doped n^+-buried layer, deposition of a 0.6 µm thick epitaxial collector layer and a standard LOCOS process for lateral isolation. In contrast to standard bipolar processing a 100 nm thick oxide layer (oxide I) is deposited in the active emitter-base region of the NPN transistors, followed by the deposition of a p-type doped poly layer (poly I). The active transistor area is opened by a RIE-process with an etch stop on the 100 nm oxide below the poly (width of the opening: 0.5 µm). A nitride spacer prevents the deposition of SiGe at the sidewalls of the poly layer. The oxide I layer below the poly I layer is removed by wet chemical etching and - by adjusting the overetch - a 100 nm undercut of the poly I is formed. The opening of the oxide I layer defines the area of the self-aligned base-collector junction.

The SiGe base layer is deposited by selective epitaxy with a monocrystaline growth mode at the Si-substrate, a polycrystaline growth at open poly-Si surfaces and an insitu boron doping. The SiGe/Si-deposition includes a layer with constant Ge content, a Ge-profile graded towards the emitter and a Si-cap. During epitaxial growth, the base contact is formed. However, there is no direct contact of the poly I layer to the substrate in order to reduce the parasitic base-collector capacitance.

After SiGe epitaxy, the nitride spacer on the sidewall is removed and a composite spacer is formed to reduce emitter width from 0.5 µm to a self-aligned effective width of 0.25 µm. After spacer formation an insitu arsenic doped poly II layer is deposited and structured to form the emitter. Using an oxide hard mask, deep trench grooves are etched to a depth of 4.5 µm after finishing the front-end process. The trenches are filled with thick intermediate BPSG oxide. Finally, an emitter Drive In is done by rapid thermal annealing at about 1000 °C.

Figure 1 presents a SEM cross section of the NPN transistor with deep trench, figure 2 a SEM cross section of the base region (double-poly self-aligned emitter-base technology) and figure 3 SIMS profiles of germanium, boron and arsenic.

In order to minimize variations of electrical parameters, process control on a nanometer scale is necessary. For example, the position of the pn-junction with respect to the Ge grading has a strong impact on variations of current gain. On the other hand, this position is mainly determined by the epitaxial growth rate (thickness of Si cap and Ge grading) and therefore by substrate temperature. However, the substrate temperature depends on chamber conditions and layout. Especially, for applications with a large number of different reticles, an inline method for process control is necessary, which allows investigations of the growth process on product wafers with high accuracy. Additionally, for a mass production, operators should be able to perform this method. In the case of a selective growth process, layer thickness can be measured by profilometry, which is a well established inline method in the case of Si processing (layer thickness is calculated from the step height between field oxide regions and regions with exposed Si-surface before and after the epitaxial growth). Figure 5 and 6 present measurements of layer thickness and

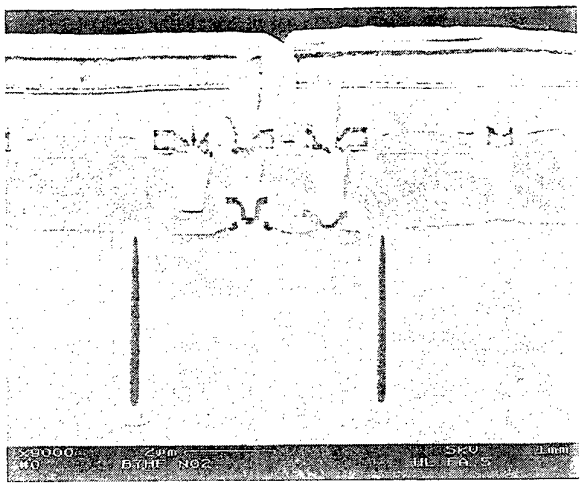

Fig. 1: SEM cross section of an NPN transistor area with deep trench isolation.

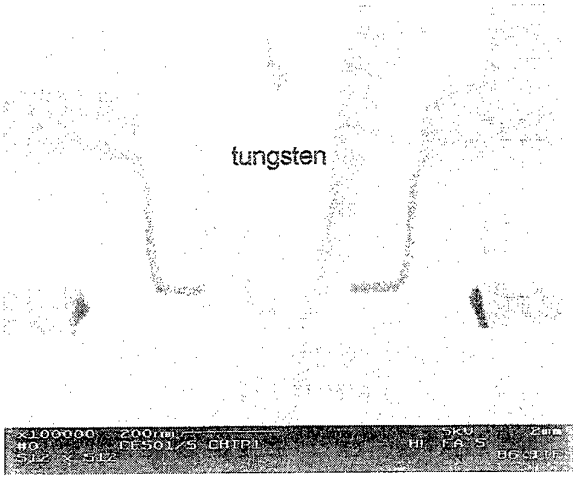

Fig. 2: SEM cross section of the base region (SiGe NPN transistor with double-poly self-aligned emitter-base technology; SiGe base layer grown by sel. epi.).

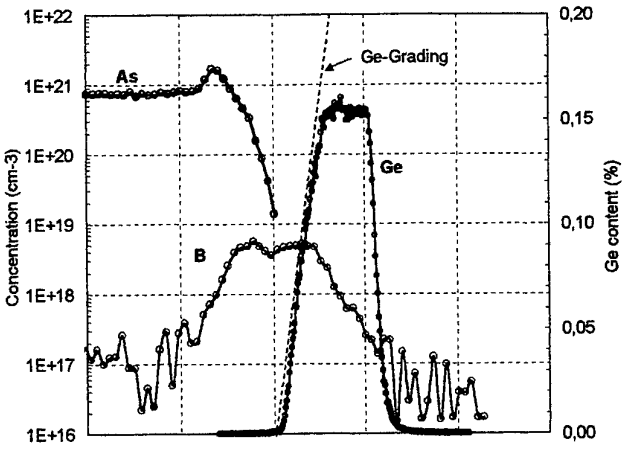

Fig. 3: SIMS profiles of Ge, B and As of a SiGe NPN transistor (process flow completely performed).

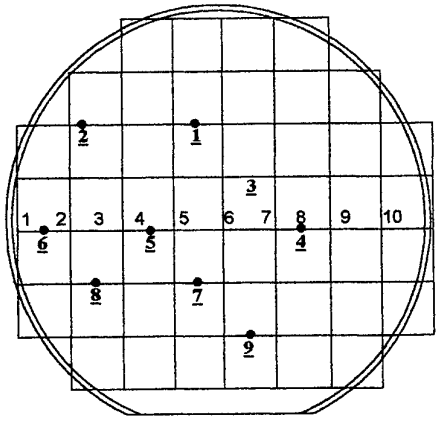

Fig. 4: Positions for measurements of layer thickness (positions 1-10) and of current gain (positions **1**-**9**)

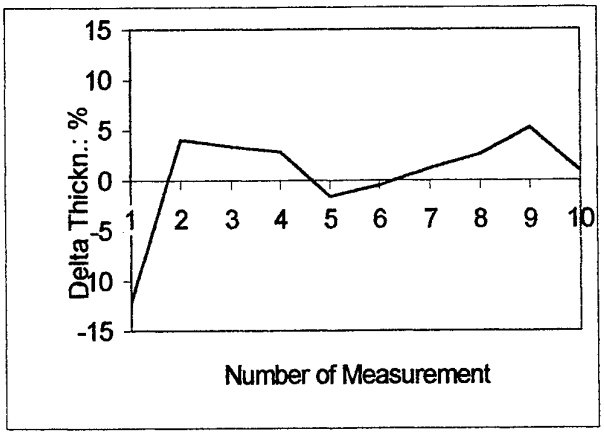

Fig 5: Variation of the epitaxially grown layer thickness across a 6 inch wafer (positions of measurements at the center of the wafer, parallel to the flat; compare fig. 4: points 1-10)

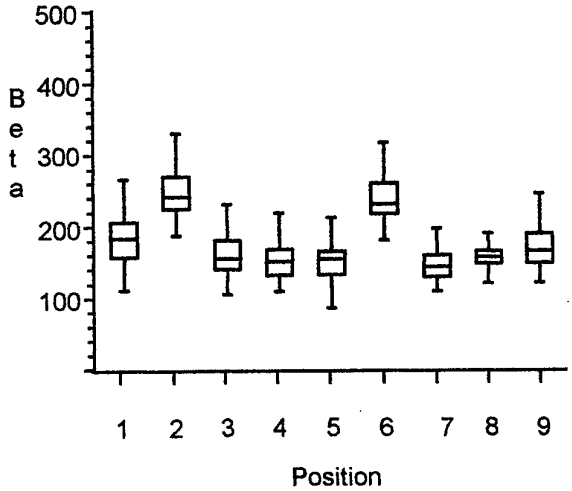

Fig 6: Variation of the current gain for 50 wafers with identical process flow (one lot); positions of measurements as described in figure 4 (points **1** – **9**).

High Speed Applications of HBTs

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M. Wojtowicz, E. Kaneshiro, K. Sato, G. Leslie, and H.C. Yen

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ABSTRACT

The performance and cost advantages of our gallium arsenide (GaAs) based Heterojunction Bipolar Transistor (HBT) technology has enabled several high volume commercial applications. TRW is currently delivering over 4 million MBE based HBT integrated circuits per month for low cost commercial wireless applications, as well as for high performance high reliability defense avionics, ground, and space applications. Indium Phosphide (InP) based HBT technology has several enabling advantages over GaAs HBTs for commercial communication applications, in particular for high efficiency cellular power amplifiers, mmW LMDS system power amplifiers, OC-768 40 GBPS fiber-optic communications, and signal processing ICs.

Cellular telephone power amplifiers have a combination of very stringent performance requirements including high power added efficiency, and low off leakage for long talk time and standby time, high breakdown voltage for use, and low implementation cost. InP HBT offers unprecedented performance over GaAs HBT technology. We will also present some measured device results including 3 volt PAE > 85% and 1 volt PAE > 65%. We will also present the economic advantages of InP HBT technology that are criticalfor this market.

Another application for InP HBT technology is high-speed fiber-optic circuits including single wavelength OC-768, 40 GBPS for internet backbone broadband data transmission. InP HBTs have advantages for several key front-end component blocks

including transimpedance amplification, gain control, clock and data recovery, modulator drivers, and high speed MUX and DMUX functions. A key parameter is switching speed and we have demonstrated frequency dividers operating beyond 70 GHz.

Our final presentation will further elaborate on the intrinsic performance advantages of InP, recent performance breakthroughs, InP technology status, InP manufacturing, and future trends of InP based HBT technology for defense and commercial applications.

MMIC, Mixed-signal, and Lightwave-Circuit Applications of GaAs HBTs

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It has been argued that GaAs is only good for RF power and optical devices. In the present technology landscape, GaAs certainly is the incumbent heavyweight in both these areas, but also finds employment in high-speed routing and mixed-signal applications such as multiplexers, crossbar switches, and ADCs.

Driven by "natural" applications in power and optical devices, GaAs technology will continue to be developed to provide improved performance in the commercial market. The advent of commercial InGaP/GaAs HBT technology may allow HBTs to be scaled aggressively and remain viable for in the relatively smaller light-wave and mixed-signal markets. In the present talk we will review the state-of-the-art in GaAs HBT technology, highlight some of the reasons why GaAs HBTs have been successfully applied for commercial RF, mixed-signal, and lightwave circuits, and finally, explore avenues for continued selection, as higher performance is required by the next-generation components

Reliability of InGaP and AlGaAs HBT

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The long-term reliability of HBTs continues to be a subject of great interest due to the increased acceptance of HBT in a wide range of applications. The most demanding requirements for long-term reliability include high-performance microwave instrumentation, X-band radar, and lightwave communication (OC-192). A dramatic increase in the long-term reliability performance was observed in GaAs-based HBTs as the AlGaAs emitter material was replaced with InGaP [1-3]. A significant improvement in the long-term reliability was also observed in AlGaAs emitter HBTs as the turn-on voltage was lowered. [4]

The typical failure mechanism in HBT devices under high current and high temperature long-term reliability testing is a significant increase in the base current at low current bias. One of the limiting factors in obtaining MTTF values in InGaP HBTs is the long time required to promote failures in the HBT devices. Furthermore, a large sample size is necessary to extract a meaningful MTTF. Significant increases in the stress current density, as high as 180 kA/cm^2, have been used to promote failures and obtain an MTTF within a reasonable amount of time [5]. At these high current densities, the device failure is rapid, with the dc current gain saturating at unity (Fig.1). The failure time distribution (TTF) at 50% dc current gain reduction for a lot size of 832 devices (30 wafers) is shown in Fig. 2. A few devices failed immediately, presumably due to the handling of the devices. However, many devices exceeded 2000 hours in TTF, even at these very high current densities. The reproducibility and robustness of InGaP/GaAs HBTs are highlighted by the large number of devices represented in this data, spanning many epitaxial wafer and process lots.

An attempt to predict the MTTF of AlGaAs and InGaP HBTs using a simple model based upon fitting the initial Gummel plots of large area devices was made [4]. Degradation of the HBT was assumed to occur near the base/emitter junction and it corresponded to an increase in the trap density within the depletion region. The model is based upon an estimation of the increase in trap defect density at the base/emitter junction, which is further related to the hole injection component of the base current via the hole barrier height and the turn-on voltage Vbe. A 5x increase in the experimental TTF was observed in $Al_{0.28}Ga_{0.72}As$ HBTs with a lower turn-on Vbe (53 mV lower at Jc = 1.8 A/cm^2), and the simulated results are shown in the solid lines (Fig.3). The lower Vbe device contained a lower effective conduction band spike at the base/emitter junction, which was obtained by properly grading the base/emitter interface. The hole injection component of the base current was estimated to be reduced by a factor of 7 in the low Vbe HBT device in comparison to the high Vbe device. An order of magnitude improvement in the reliability of InGaP HBTs was projected based upon the above model when using an activation energy (Ea = 0.63 eV) that has been observed for InGaP HBTs [3].

Both experimental and simulated results suggest that the emitter material is primarily responsible for determining the long-term reliability characteristics of GaAs-based HBTs. The combination of a high effective hole barrier and a low Vbe are highly desirable for long-term reliability characteristics. Emitter materials such as InGaAlP and higher AlGaAs compositions may demonstrate excellent reliability characteristics at high temperatures and high current densities.

[1] T. Takahashi et. al. Proc IEDM, 191 (1994).
[2] N. Pan et. al. Elec. Dev. Lett. 19, 115 (1998).
[3] T. S. Low et. al. Proc. GaAs IC Symp. 153 (1998).
[4] Welser et. al. to be published in Proc. GaAs Mantech 2000.
[5] B. Yeats et. al. to be published in Proc. GaAs Mantech 2000.

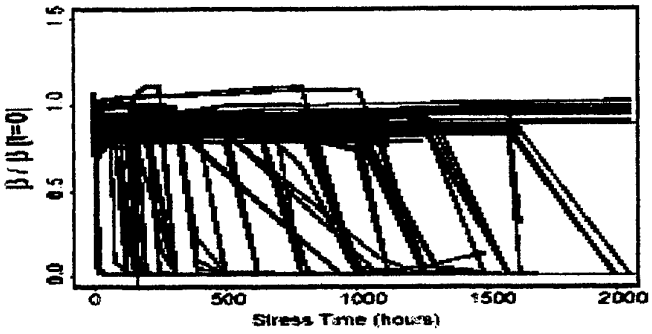

Fig. 1. Normalized dc current gain drift for a sample size of 500 devices. The reliability test conditions were, Tj = 334 C, Vce = 5.0 V, Jc = 180 kA/cm^2 (L = 2 x 2 um^2) [Ref. 5].

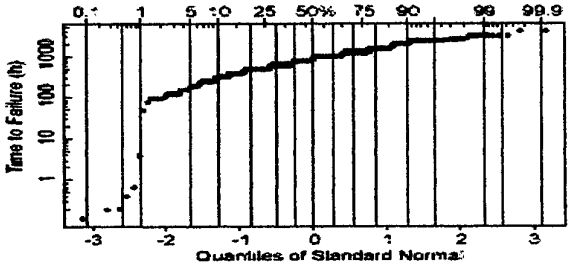

Fig. 2. The failure time distribution for 50% dc current gain drift for 832 devices. The reliability test conditions were, Tj = 334 C, Vce = 5.0 V, Jc = 180 kA/cm^2 (L = 2 x 2 um^2) [Ref. 5].

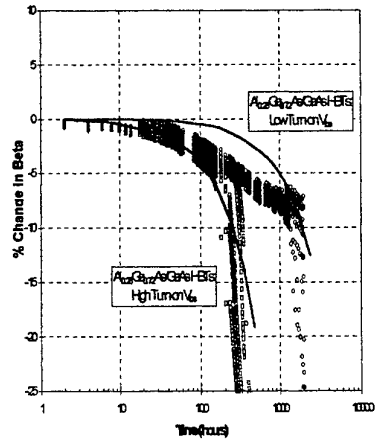

Fig. 3. Long-term reliability characteristics (10 devices) from two different sets of AlGaAs HBT. The testing conditions were Tj = 260 C, Vce = 7.0 V, and Jc = 48. 5 kA/cm^2 (L = 1.7 um x 19.7 um x 4). The solid lines are simulated results. The TTF increased from 400 to over 2000 hours [Ref. 4].

HBT Power Amplifier MMICs for Hand-held Systems

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ABSTRACT

Highly reliable and reproducible mass production of AlGaAs/GaAs HBT MMICs for handy phones is reported in this paper. Design of the thermal structure and the active feedback circuit for high VSWR operation, which are the key technologies for GSM application, are also briefly reviewed.

INTRODUCTION

Corresponding to the nowadays rapidly increasing demands for personal wireless communication systems, the power amplifiers for handy phones of low cost, small chip-size, and high power efficiency with low voltage single power supply are required. GaAs based HBT amplifier is one of the powerful candidate, because of its high power density operation at low single voltage with high efficiency, and the cost effective wafer process.

The GSM phone system is most powerful in the world wide wireless communication market. The power amplifier for GSM handset has to respond to the requirements of multi-band operation, more price down, high VSWR operation by excluding the isolator from the antenna, and so on. The most fundamental technologies to realize the HBT power amplifier for GSM application are the heat treatment[1, 2], bias circuit design[3], and burnout protection for high VSWR operation[4]. We currently produce more than 1 million Dual Band HBT MMIC chip sets per month for GSM phones. In this paper, we briefly review our thermal structure design, active feedback circuit for high VSWR operation , and the excellent reproducibility of AlGaAs/GaAs HBT mass production.

HBT DEVICE STRUCTURE

A. Design of Thermal Structure

To realize the multi finger HBT power amplifier in small chip-size, we designed the thermal structure based on the three dimensional simulation of thermal flow. Figure 1 shows our thermal shunt structure with Au plated air-bridge. The thermal resistance of each finger ($4\mu m \times 20\mu m$) is 40% reduced with this structure. The finger layout was also optimized based on the three dimensional thermal simulation.

B. Active Feedback Circuit for High VSWR Operation

The burnout failure of HBT fingers during the high VSWR operation under the load-side mismatched conditions is the thermal runaway phenomena caused by the hole feedback effect enhanced by the base -collector avalanche break down at the expanded load line under the mismatched conditions. To suppress the hole feedback effect, we designed the active feedback circuit based on the load line simulation as shown in figure 2. With the active feedback circuit, we have no burnout failure even under the 10:1 VSWR at 5V operation.

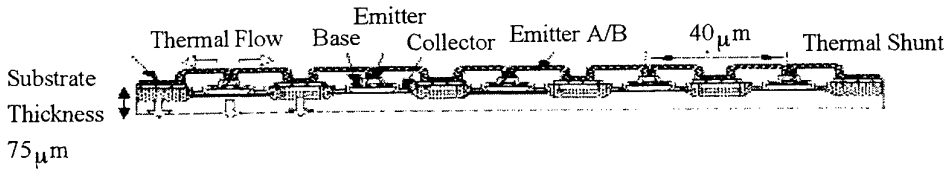

Figure 1 Thermal Structure for AlGaAs/GaAs HBT PA

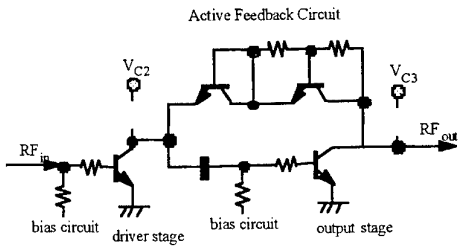

Figure 2 Active Feedback Circuit

REPRODUCIBILITY IN MASS PRODUCTION

To deliver the reliable HBT MMICs in large quantity, the controllability of the epitaxial quality and the wafer process reproducibility must be established.

Figure 3 (a)-(c) show the trends of the fundamental parameters of HBTs in 350 lots as examples of mass production reproducibility. Each process lot contains 24 wafers. Every parameter is well controlled in the mass production stage.

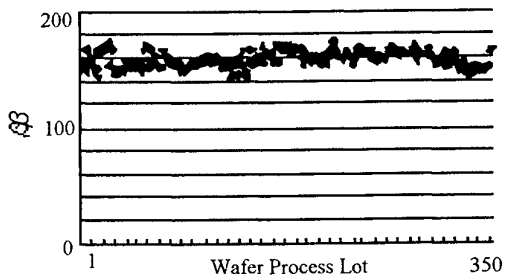

Figure 3 (a) β Trend

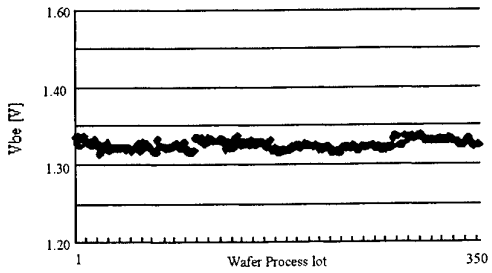

Figure 3 (b) Vbe Trend

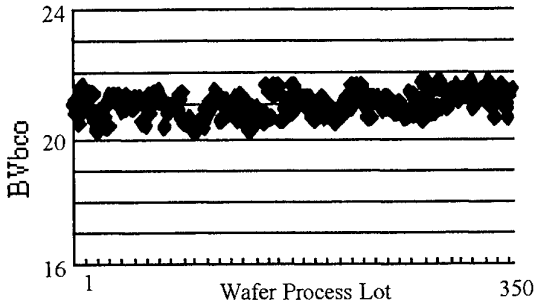

Figure 3 (c) BVbcoTrend

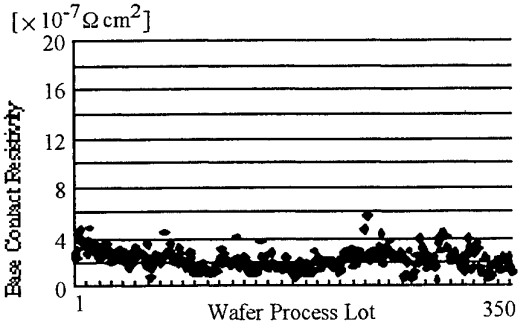

Figure 3 (d) Base Contact Resistivity Trend

RFERENCES

1) R.Hattori et al., "Three-Dimensional Modeling of Thermal Flow in Multi-Finger High Power HBTs", IEEE MTT-S Digest, 461, 1995

2) T.Shimura et al., "High Efficiency AlGaAs/GaAs power HBTs at low supply voltage for digital cellular phones," IEICE Trans. Electronics, vol..E80-C, No.6, 740, 1997

3) K.Yamamoto et al., "A 3.2-V Operation Single-Chip AlGaAs/GaAs HBT MMIC Power Amplifier for GSM900/1800 Dual-Band Application", IEEE MTT-S Digest, 1397, 1999

4) S.Suzuki et al., "A New Approach to Prevent The Burnout Under Mismatching Load Conditions in High Power NBT," 29th European Microwave Conference, Proceeding, 117, 1999

InGaP/GaAs HBTs for portable wireless applications

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GaAs-based HBTs have several features that make them suitable for transmitter power amplifiers in portable wireless communication systems. These include a single bias supply, high linearity, high efficiency even under low voltage operation, and high power-handling capability per unit chip area, as well as semi-insulating substrates that allow convenient MMIC fabrication. Among the GaAs-based HBTs, InGaP/GaAs HBTs are of great interest because of greater reliability and ease of fabrication using selective etching. This paper discusses about design and fabrication issues on InGaP/GaAs HBTs for low-voltage personal cellular phones.

The crystalline properties of InGaP layers vary with growth conditions of MOCVD in association with the ordered structure. An ordered InGaP emitter reduces the collector offset voltage, compared to a disordered InGaP emitter, due to reduced conduction band discontinuity at the InGaP/GaAs heterointerface. However, the ordered structure induces carrier traps at the interface, and this significantly increases base leakage current at low current densities in some emitter structures. Care should be taken in the epitaxial growth of the GaAs/ordered-InGaP interface to maintain high current gain even at low current densities.

Wide bandgap of InGaP layers closely relates with fairly good dc characteristics of the InGaP/GaAs HBTs. The InGaP emitter structure markedly reduces the surface recombination at the emitter edge, making the emitter size effect, which is often a serious problem in AlGaAs/GaAs HBTs, practically negligible. The higher energy-gap emitter structure can also suppress current gain degradation up to higher temperatures. These reduced base recombination characteristics at high current densities and elevated temperatures can also translate to high reliability in the InGaP/GaAs HBTs under forward bias stress at high temperatures.

The InGaP/GaAs HBTs that we developed for power amplifiers of low-voltage personal cellular phones have an 80-nm-thick GaAs base layer, C-doped to 4×10^{19} cm^{-3}, exhibiting a dc current gain of about 150, a collector offset voltage of 80 mV, and a collector breakdown voltage BV_{CEO} of more than 13 V. These HBTs also show no burn-in effect and excellent reliability. An MTTF extrapolated to a junction temperature of 135℃ was more than 10^8 h at a collector current density of 4×10^4 A/cm^2. Preliminary results on power performance of the InGaP/GaAs power HBTs will also be presented.

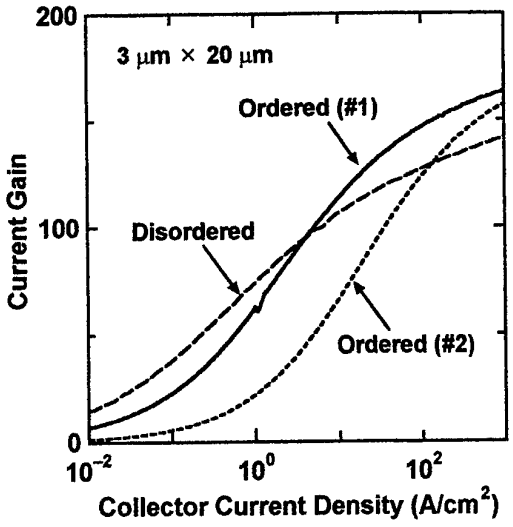

Fig. 1. DC current gain as a function of collector current density, obtained for InGaP/GaAs HBTs with ordered and disordered InGaP emitter layers. The n-GaAs/n-InGaP interface was better controlled in Sample #1 than in Sample #2.

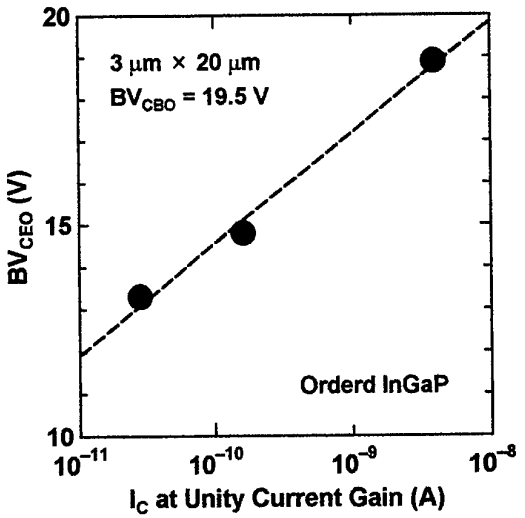

Fig. 2. Breakdown voltage BV_{CEO} vs. collector current that gives a unity current gain (h_{FE} = 1), obtained for InGaP/GaAs HBTs with the ordered InGaP structure. This shows that an increase in h_{FE} at low J_C results in a reduction in BV_{CEO}.

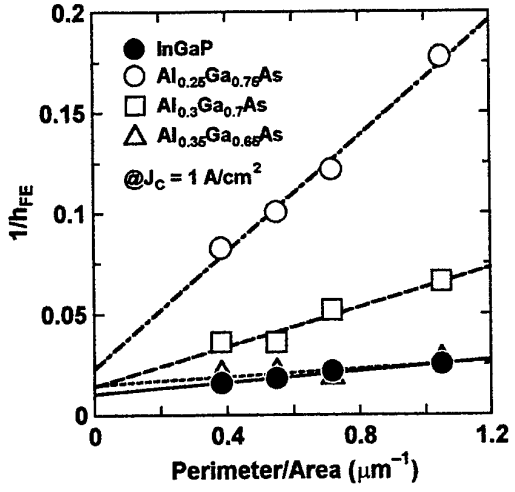

Fig. 3. $1/h_{FE}$ vs. emitter perimerter/area ratio for InGaP/GaAs and AlGaAs/GaAs HBTs with various Al composition. The emitter size effect in the $Al_{0.35}Ga_{0.65}As$ emitter HBTs was as negligible as that in the InGaP emitter HBTs, suggesting that the high enegy-gap emitter is a key to a reduction in extrinsic surface recombination.

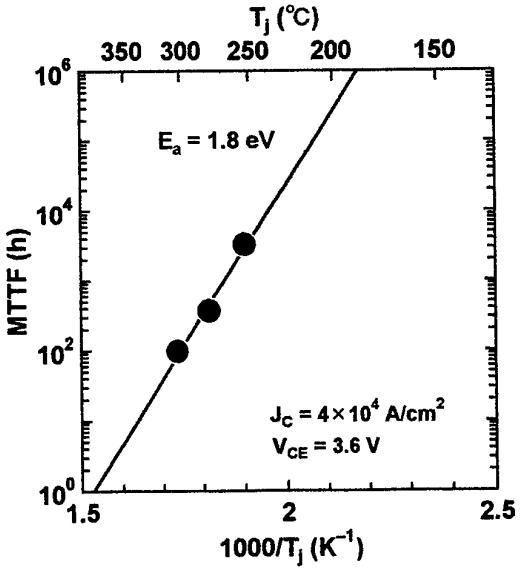

Fig. 4. Arrhenius plot of MTTF for InGaP/GaAs HBTs biased at $J_C = 4\times10^4$ A/cm^2 and V_{CE} = 3.6 V. The failure was defined as a reduction in h_{FE} to 90% of the initial unstressed value. Measurements were done at room temperature and $J_C = 3.4 \times 10^3$ A/cm^2.

Auther Index

Auther Index